Silicon Photonic OEIC for Memory Cell Information Sensing

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Abstract: We propose and experimentally demonstrate a novel scheme for simultaneous optical sensing of electric memory cell states. Results show that the effective sensing speed can be enhanced by 976 times with 100 nm spectrum ranges.

OCIS codes: (250.3140) Integrated optoelectronic circuits; (130.3120) Integrated optics devices; (130.4815) Optical switching device; (130.2790) Guided waves; (210.4680) Optical memories; (200.4650) Optical interconnects.

1. Introduction

Memory and its related products have been widely applied in many fields, especially in computers. With progress of semiconductor integrated technology, the CPU performance has been continuously improved, while the memory reading and writing speed has not improved accordingly. Several existing works are trying to link the optical interconnect into memory system [1,2], yet the memory sensing is still realized electrically. It is not able to sense more than two memory cell's information at the same time in a bit-line, as the two electrical signals will be completely mixed together and can't be distinguished. Alternatively, in the optical field, it is possible to avoid this problem. By optical WDM (Wavelength Division Multiplexing) technology, a single waveguide can transmit multiple wavelengths of light at the same time.

Recently, we had proposed and demonstrated electrically programmable optical memory circuits [3,4]. However, in this report, we propose a novel optoelectronic integration circuit (OEIC) for optical sense and transmit memory array information. The system insert microring resonator (MRR) array in a traditional memory system. Each MRR is controlled by a memory cell. Different memory cell with information 0 or 1, corresponding to different resistance. So the voltage applied to the MRR will be also different. Different current will makes the MRR resonance wavelength shift. By measuring the wavelength shift, we can know the information carried by the memory cell. In order to makes the optical signal of the MRR on a bit-line without interference in a waveguide, each MRR resonance wavelength must be different. In the receiving end, the optical information can be de-multiplexed, and converted back to the electrical signal by a photodetector array [5]. In this report, we use SONOS (Silicon-Oxide-Nitride-Oxide-Silicon) transistor [6] as the memory cell for proof-of-concept demonstration.

2. Structure, designation, experiment results and discussion

The optical circuits for sensing memory cell is illustrated in **Fig. 1(a)**. The MRR waveguide is ridged waveguide with integrated P-i-N diode. P-type and N-type dopant region are located inside and outside of MRR, respectively. The SONOS transistor directly connects with N-type slab. **Figure 1(b)** shows the optical microscope picture. The radius of MRR is 15 μm. The cross-sectional schematic that cutting through the center of MRR is shown in **Fig. 1(c)**. The ridge and slab thickness are 340 nm and 100 nm, respectively. The ridge waveguide width is 500 nm. The gap between coupling waveguide and MRR is 300 nm. The SEM picture **Fig. 1(d)** shows the top view of SONOS, and TEM picture **Fig. 1(e)** shows the cross section of SONOS. The ONO stack layers in SONOS are 2.5 nm/3.4 nm/5.5 nm, respectively.

Fig. 2(a) shows the relationship of drain current (I_D) as function of gate voltage (V_{GS}). We fix the voltage of drain and source as V_{DS}=1.25 V, and scan the gate voltage from -10 V to 10 V, then vice versa. The dashed arrows indicate the drain current changing path. We define the rising path and fall path as ON and OFF states, respectively. The curves become a loop. This is because, after high voltage in gate, the electrons tunnel through the gate oxide and are trapped in silicon nitride layer. It results in an additional voltage between source and drain, thus narrowing down the effective channel width. Therefore, even in same gate voltage, the drain current is decreased. The channel width of SONOS is 3 μm. With increase of the gate length, the drain current is deceased. The drain current difference is used to distinguish the SONOS memory states. Maximum current difference ($\Delta I_D = I_D(ON) - I_D(OFF)$) as functions of gate length are shown in **Fig. 2(b)**. The shorter the gate length is, the larger the drain current difference. Large current difference is conductive to the distinguish memory states. In considering of OFF state, the current is as smaller as better. Thus, we chose 300 nm for following experiment.

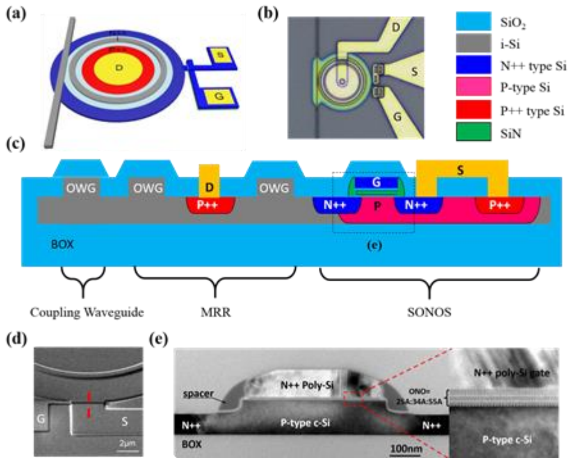

Fig. 1(a) 3D perspective view of the MRR sense SONOS state. **Fig. 1(b)** Optical microscope picture of device. **Fig. 1(c)** the cross-sectional schematic of the device. **Fig. 1(d)** the SEM picture of SONOS transistor. **Fig. 1(e)** the TEM picture of SONOS cross section and zoom in of ONO stack layer.

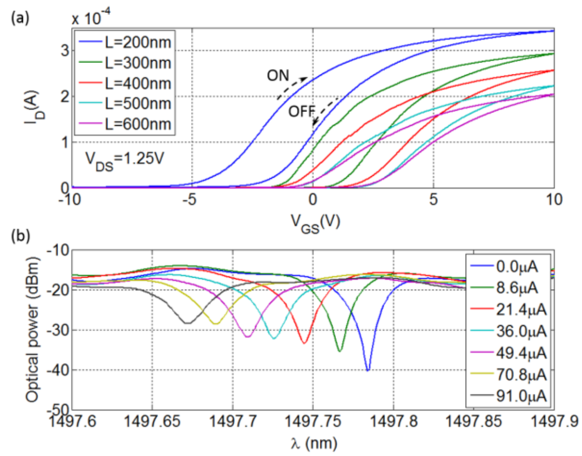

Fig. 2(a) Drain current vs. gate voltage with different gate length. The gate voltage increase from -10 V to 10 V and vice versa. The voltage of source and drain is fixed at 1.25 V. **Fig. 2(a)**. Spectrum with different drain current. The dished arrow shows the spectrum shift with current increasing.

The wavelength shift distinguashing is dependent on the detection accuracy. We assume that the wavelength shift of ON/OFF state is a FWHM, and the channel space is two times of FWHM. Since the FSR of MRR and FWHM are 6 nm and ~49 pm, respectively. An FSR can accummodate ~61 channels. In other words, we can sence 61 memory information by a single coupling waveguide simultaneously. If we adopting a wider light source, such as LED (Light-Emitting Diode) or SLD (Supper Laser Diode), the light band width can reach upto ~100 nm. we can split it into 16 bit line. Thus we can in total sense $16 \times 61 = 976$ cells at the same time. Since those 976 cell's informantion according to 976 different wavelengths, those 976 memory cell's information can be loaded in a single optical waveguide. Obeviously, higher Q-value MRRs can sense more memory cells. For example, with a MRR of 40 pm FWHM, it in principle can sense 1200 cells in simutaniusly.

3. Summary

We proposed and demonstrated a novel silicon photonic OEIC for simultaneous optical sense of electric memory cell states aiming to enhance the data-reading speed. Results show that the effective reading speed can be enhanced by 976 times with 100 nm spectrum ranges.

4. Acknowledgement

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5. References

[1] D. Brunina, C. P. Lai, A. S. Garg, and K. Bergman, "Building data centers with optically connected memory," J. Opt. Commun. Netw. 3, A40-A48 (2011)
[2] B. Hyunil et. al., "Bulk-Si photonics technology for DRAM interface," Photon. Res. 2, A25-A33 (2014)
[3] J.-F. Song, X.-S. Luo, A. E.-J. Lim, et al., "Integrated photonics with programmable non-volatile memory." Sci. Rep. 6:22616 (2016)
[4] J.-F Song, A. E.-J. Lim, X. -S. Luo, et.al., "Silicon photonic integrated circuits with electrically programmable non-volatile memory functions," Opt. Express 24(19) 21744-21751 (2016)
[5] L. Chen and M. Lipson, "Ultra-low capacitance and high speed germanium photodetectors on silicon," Opt. Express 17, 7901-7906 (2009)
[6] R. Bez, E. Camerlenghi, A. Modelli, and A. Visconti, "Introduction to Flash Memory," Proceedings of The IEEE, 91(4), 489-502 (2003)