Solution Processed Top-Gate High-Performance Organic Transistor Nonvolatile Memory With Separated Molecular Microdomains Floating-Gate

Chao Wu, Wei Wang, and Junfeng Song

***Abstract*— In this letter, a top-gate high-performance floating-gate organic field-effect transistor nonvolatile memory (FG-OFET-NVM), where the four-layer stacked core architecture is processed by a successive solution spin-coating method, is demonstrated. The floating-gate layer is prepared by spin-coating from a blend solution consisting of poly(styrene) (PS) and 6,13-bis(triisopropylsilylethynyl)pentacene (TIPS-Pen). As a result of phase separation, TIPS-Pen aggregates and forms many separated microdomains, which uniformly distribute in the matrix of PS as the charge-trapping sites. The optimal FG-OFET-NVM exhibits excellent memory characteristics, with a large memory window of 26 V, a desired reading voltage of 0 V, a memory ON/OFF ratio larger than 3500, programming/erasing switching endurance over 500 cycles, and good charge-storage retention with a memory ON/OFF ratio larger than 10^3 over 5000 s.**

***Index Terms*— Organic field-effect transistor memory, molecular floating-gate, successive solution processing.**

I. Introduction

FLOATING-GATE organic field-effect transistor nonvolatile memory (FG-OFET-NVM) has attracted great interest and is considered a promising candidate for next-generation organic flash memory due to its simple device structure of a single-transistor, nondestructive read-out, compatibility with complementary logic circuits and their potential application as flexible or stretchable charge storage media [1], [2]. The memory mechanism is attributed to the charge trapping and de-trapping in/from the floating-gate at the supplied programming and erasing voltages (V_P and V_E), respectively. Many efforts have been taken on the development of the materials and the microstructures of the floating-gates to achieve stable and reliable nonvolatile memory characteristics, such as various metal nanoparticles [2]–[12], polymer nanoparticles [13], and molecular semiconductors [14]–[16]. The core architecture of a standard FG-OFET-NVM consists of a semiconductor layer, tunneling layer, floating-gate layer, and blocking layer in addition to three terminal electrodes. In most of the previously reported FG-OFET-NVMs, at least one layer from the four-layer stacked core architecture, such as the floating-gate layer [2]–[4] or the organic semiconductor layer [5]–[16], was prepared by vacuum thermal evaporation to avoid damaging the underlying film. Vacuum thermal evaporation is a technique with high energy consumption and is therefore undesirable for the continuous processing and the large area and low-cost fabrication of memories. On the other hand, the top-gate configuration is more desirable than the bottom-gate configuration in FG-OFET-NVMs, because the auto-encapsulation of air-sensitive organic semiconductors by the overlaid gate insulator and gate electrode improves the device-operating stability [2]–[4], [17]. To date, there have been very few reports of top-gate FG-OFET-NVMs containing the entire four-layer stacked core architecture that was fabricated using exclusively solution-processing technique [18].

In this letter, we propose and prepare the floating-gate layer by employing both the molecular semiconductor 6,13-bis(triisopropylsilylethynyl)pentacene (TIPS-Pen) and the polystyrene (PS) based on previous work that utilized both materials dissolved in the same solvent to prepare an organic field-effect transistor (OFET) by taking advantage of the resulting phase-separation with spin-coating [19]. Additionally, we fabricate a top-gate FG-OFET-NVM, of which the four-layer core architecture is processed by a successive spin-coating method. As a result, an excellent FG-OFET-NVM is achieved, with a large memory window of 26 V, a desired reading voltage of 0 V, reliable programming/erasing (P/E) switching endurance more than 500 cycles, and very stable charge storage retention capability with a memory on/off ratio larger than 10^3 over 5000 s.

II. Device Structure and Fabrication

Figure 1 shows the three-dimensional (3D) structure of our FG-OFET-NVM and the chemical structures of the materials

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C. Wu is with the State Key Laboratory of Integrated Optoelectronics, College of Electronic Science and Engineering, Jilin University, Changchun 130012, China, and also with the School of Electric and Information Engineer, Zhongyuan University of Technology, Zhengzhou 450007, China.

W. Wang and J. Song are with the State Key Laboratory of Integrated Optoelectronics, College of Electronic Science and Engineering, Jilin University, Changchun 130012, China (e-mail: wwei99@jlu.edu.cn).

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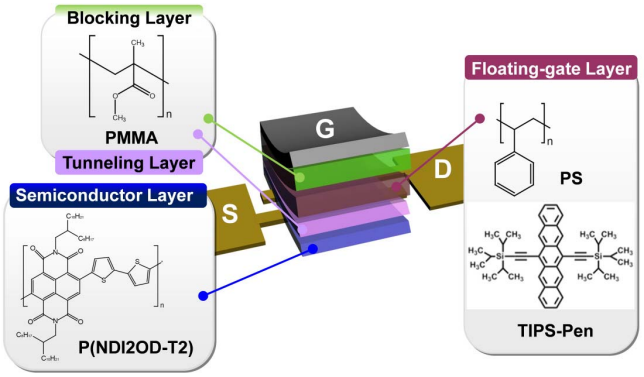

Fig. 1. Three-dimensional structure schematic of the present FG-OFET-NVM and the chemical structures of the materials used in the core architecture.

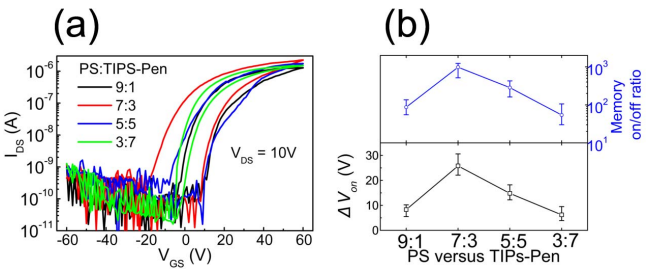

Fig. 2. (a) Transfer characteristics of the FG-OFET-NVMs with different ratios of PS to TIPS-Pen in the floating-gate layers. (b) Both ΔV_{on} and memory on/off ratio as functions of the ratio of PS to TIPS-Pen in the floating-gate layers.

used in each layer. Au film (30 nm) was thermally evaporated on the surface of a 300-nm thick SiO_2 insulator coated Si substrate as source/drain electrodes through a shadow mask. The channel length (L) and width (W) were 100 and 1000 μm, respectively. A 50-nm thick polymer poly{[N,N'-bis(2- octyldodecyl)-naphthalene-1,4,5,8-bis(dicarboximide)-2,6-diyl]-alt-5,5'-(2,2'-bithiophene)} [P(NDI2OD-T2)] was spin- coated from a toluene solution onto the source/drain electrodes to serve as the semiconductor layer. A 35-nm thick poly(methyl methacrylate) (PMMA) tunneling layer was subsequently spin-coated onto the P(NDI2OD-T2) film from a butyl acetate (BA) solution at a concentration of 0.5 wt%. 50-nm thick floating-gate layers, consisting of polymer PS and TIPS-Pen at different mass proportions of 9:1, 7:3, 5:5, and 3:7, were then spin-coated onto the PMMA tunneling layer from their blend solution in chlorobenzene with a concentration of 1 wt%. Next, a 330-nm thick PMMA blocking layer was spin-coated onto the floating-gate layer from its 2-ethoxyethanol (2E) solution with a concentration of 5 wt%. Upon sequential preparation of each layer, post-thermal annealing was employed to remove the residual solvents at 100° C. The annealing time was of 10, 10, 10, and 120 min, respectively. 100-nm thick Al gate electrodes were thermally deposited on the surface of the PMMA blocking layer through a shadow mask. The devices were patterned by oxygen plasma etching to finish the fabrication, with the Al gate electrodes as the shadow mask. The fabricated memories were characterized with a semiconductor parameter analyzer (Keithely 4200 SCS) in the ambient atmosphere at room temperature. The thicknesses of all of the films were measured using a Dektak 6 Surface Profiler. The surface morphologies of the semiconductor layer, the tunneling layer, and the floating-gate layer were investigated by a tapping-mode atomic force microscopy (AFM) (Dimension Icon, Bruker Co.).

III. Results and Discussion

The morphologies of the spin-coated semiconductor layer, tunneling layer, and floating-gate layers are investigated by AFM measurement. Both the semiconductor layer and the PMMA tunneling layer exhibited uniform and smooth surface morphologies. During the spin-coating of the blend solution consisting of PS and TIPS-Pen, phase-separation occurred, resulting in separated TIPS-Pen microdomains uniformly distributed in the PS matrix, in the case of the low composition of TIPS-Pen. In contrast, phase inversion occurred when the proportion of TIPS-Pen further increased to 50%, which resulted in that many PS microdomains embedded in the TIPS-Pen matrix. The surface roughness of these floating layers increased with the increasing proportion of TIPS-Pen, due to its obvious aggregation.

In the floating-gate layers, TIPS-Pen microdomains act as the charge-trapping sites while dielectric PS is employed to avoid the lateral tunneling of the trapped charges among the TIPS-Pen microdomains. It is noted that the orthogonal solvents (BA and 2E) were used to avoid damaging the morphology and microstructure of the underlying films during the spin-coating of the subsequent layers [17]. The impact of spin-coating the floating-gate layer on the PMMA tunneling layer was negligible, as demonstrated by good memory performances and the relevant experiment that the spin-coated 40-nm thick PMMA film on the Si/SiO_2 substrate could maintain smooth and free pin-hole morphology after quickly spin-coating pure chlorobenzene solvent on its surface. As for our present FG-OFET-NVM, employing full solution processing to build its four-layer stacked core architecture provides prominent merits in terms of low-cost, low-temperature, and successive fabrication when compared with other previous works [2]–[16].

Figure 2a shows the linear transfer characteristics of our FG-OFET-NVMs with different proportions of TIPS-Pen in the floating-gate layers. For all devices, ambipolar charge-transport characteristics were obtained in all devices with a strong electron mobility of about 0.1 cm^2/Vs and a weak hole mobility of $10^{-4} \sim 10^{-3}$ cm^2/Vs in the linear range, independent of the proportion of TIPS-Pen. The memory window (ΔV_{on}) is defined as the difference of the turn-on voltages (V_{on}) after P/E operations. Here, V_{on} was defined as the V_{GS} where the I_{DS} increased to 1.0 nA. Both the ΔV_{on} and the memory on/off ratio obviously depended on the proportion of TIPS-Pen in the floating-gate layers because the stored charge density depended on the TIPS-Pen microdomain density in the floating-gate. The largest ΔV_T and highest

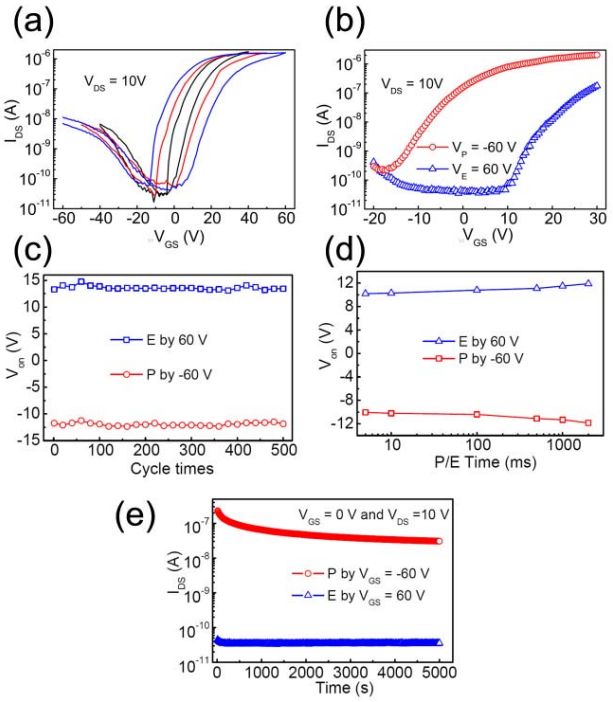

Fig. 3. (a) Transfer characteristics of the optimal FE-OFET-NVM operating at different bidirectional V_{GS} sweeping ranges. (b) The transfer characteristics of the FE-OFET-NVM after P/E operations. Record of V_{on} at both 1 and 0 states (c) of 500 cycles for switching behavior, and (d) as the function of P/E pulse time in the optimal FG-OFET-NVM. (e) The nonvolatile characteristics of the optimal FE-OFET-NVM.

memory on/off ratio were simultaneously achieved in the FE-OFET-NVM with a floating-gate consisting of PS: TIPS-Pen at 7:3, which was considered to be the optimal device.

Figure 3 shows the transfer characteristics of an optimal FE-OFET-NVM operating in different gate-source voltage (V_{GS}) sweeping ranges. The clockwise hysteresis loop enlarged in bi-direction with the increasing V_{GS} from ± 40 to ± 60 V, indicating that either electrons or holes could be injected and trapped in TIPS-Pen from the P(NDI2OD-T2) at the supplied positive or negative V_{GS}, respectively. By supplying a V_P pulse of -60 V for 5 ms, the transfer curve was negatively shifted with a V_{on} of -12.5 V (denoted as 1 state), due to holes injecting and trapping in the floating-gate from the channel (Fig. 3b). At the supplied V_E pulse of 60 V for 5 ms, electrons were injected into the floating-gate from the channel, which overwrote the previous trapped holes in the floating-gate. The trapped electrons in the floating-gate induced a built-in electric field, which resulted in a positive-shifted transfer curve with a V_{on} of 14.2 V (denoted as 0 state), as shown in Fig. 3b. As a result, a large ΔV_{on} of 26.7 V was achieved at the V_P/V_E of ± 60. Thanks to the sufficiently large negative and positive V_{on} at the 1 and 0 states, respectively, the reading voltage ($V_R = V_{GS}$) could be set as 0 V, which is a desired value for the lowest power consumption and the minimal external influence on the reading state. At V_R of 0 V, the achieved memory on/off ratio was larger than 3500. At the supplied circular P/E operations, the V_{on} of our memory switched well between the 1 and 0 states, and maintained well with a slight fluctuation over 500 switching cycles, indicating good operating reliability (Fig. 3c).

In another fresh memory with an optimal composition, the extracted V_{on} at both the 1 and 0 states slightly changed with the increasing P/E pulse time from 5 ms to 1 s (Fig. 3d), indicating that the P/E pulse time of 5 ms was enough for the P/E operations, i.e., our memory possessed the capability to be quickly programmed and erased. Figure 3e shows the measured nonvolatile properties in our floating-gate memory. After supplying a V_P/V_E of ± 60 V, the reading current (I_{DS-1} and I_{DS-0}) at the 1 and 0 states were measured as a function of time at the reading state of $V_R = 0$ V and $V_{DS} = 10$ V. During the measuring time of 5000 s, I_{DS-1} degraded slightly, while the I_{DS-0} was almost unchanged. The memory on/off ratio was always larger than 10^3 during the measuring time of 5000 s, indicating a promising application of our fabricated floating-gate transistor as a nonvolatile memory.

IV. Conclusion

In summary, we have developed an FG-OFET-NVM by a full solution processed method to build its four-layer stacked core architecture. With an optimal floating-gate consisting of PS versus TIPS-Pen at 7:3, a high-performance FG-OFET-NVM was achieved, with a large memory window of 26 V, a desired V_R of 0 V, reliable P/E switching endurance of more than 500 cycles, and stable charge storage-retention capability with the memory on/off ratio larger than 10^3 over 5000 s.

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