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Molecular floating-gate organic nonvolatile memory with a fully solution processed core architecture

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In this paper, we demonstrated a floating-gate organic thin film transistor based nonvolatile memory, in which the core architecture was processed by a sequential three-step solution spin-coating method. The molecular semiconductor 6,13-bis(triisopropylsilylethynyl)pentacene (TIPS-Pen) distributing in the matrix of polymer poly(styrene) (PS), acting as the floating-gate and tunneling layer, respectively, was processed by one-step spin-coating from their blending solution. The effect of the proportion of TIPS-Pen in the matrix of PS on the memory performances of devices was researched. As a result, a good nonvolatile memory was achieved, with a memory window larger than 25 V, stable memory endurance property over 500 cycles and retention time longer than 5000 s with a high memory ratio larger than 10^2, at an optimal proportion of TIPS-Pen in the matrix of PS. *Published by AIP Publishing.* [http://dx.doi.org/10.1063/1.4971187]

The floating-gate organic thin film transistor based nonvolatile memory (FG-OTFT-NVM) has attracted great attention as a promising candidate for the next-generation organic flash memory due to its simple device structure of single-transistor, non-destructive read-out, massive memory capacity, compatibility with complementary logic circuits and their potential application as flexible or stretchable charge storage media.[1,2] The core architecture of a standard FG-OTFT-NVM is consisted of the semiconductor layer, tunneling layer, floating-gate layer and blocking layer, besides three terminal electrodes. The operation mechanism of this type memory is that the charges are trapped and detrapped in/from the floating-gate at the supplied programming voltage (V_P) and erasing voltage (V_E), respectively. In the last decade, great efforts have been focused on the research of the floating-gate layer, including the proper selection of materials as the floating-gate layer (such as Au, Ag, Cu, Al, reduced graphene oxide and molecular semiconductors)[3–10] and the utilization of various processing technologies (such as vacuum thermally evaporation,[11] electrostatic self-assembly,[12–14] templated synthesis with block copolymer,[5] microcontact printing[15] and solution spin-coating[16]) to build the nano-structural floating-gate for realizing non-volatile memory characteristics. Up to now, most of the reported FG-OTFT-NVMs used a bottom-gate structure and were processed by multiple technologies to build the core architecture of the memory, in which the semiconductor layers were prepared by high vacuum thermally evaporation.[4–16] Not to mention high vacuum thermally evaporation, which is undesirable for continuously processing, large area and low-cost memories, top-gate structure is more desirable for reliable operation due to the auto-encapsulation of air-sensitive organic semiconductors by the overlaid gate insulator and gate electrode.[2,3] In a few reported top-gate FG-OTFT-NVMs, the floating-gate layers were prepared by vacuum thermally evaporation.[3,17] For the perspective of the future industrial production, the solution processing is desired for the fabrication of a multilayer structural FG-OTFT-NVM due to low-cost and successive processing. But, the reports about top-gate FG-OTFT-NVM with a multilayer core architecture fabricated by a fully solution processing method were a few.[18]

In this paper, we demonstrated the top-gate structural FG-OTFT-NVMs, in which the core architecture was prepared by a simple three-step solution processing method. The nano-structural molecular semiconductor 6,13-bis(triisopropylsilylethynyl)pentacene (TIPS-Pen) was well distributed in the matrix of polymer poly(styrene) (PS) by one-step spin-coating from their blend solution. The TIPS-pen and PS acted as the floating-gate and tunneling layer, respectively. By selecting an optimal proportion of TIPS-Pen versus PS, stable and reliable nonvolatile memories were achieved on both rigid and flexible substrates.

On the surface of the Si/SiO_2 (300 nm) substrates, Au film (30 nm) was thermally evaporated as source/drain (S/D) electrodes through a shadow mask. The channel length (L) and width (W) were 100 and 1000 μm, respectively. A 50 nm thick poly{[N,N′-bis(2-octyldodecyl)-naphthalene-1,4,5,8-bis(dicarboximide)-2,6-diyl]-alt-5,5′-(2,2′-bithiophene)} P(NDI2OD-T2) was spin-coated on the substrates with the S/D electrodes from its toluene solution, acting as the semiconductor layer. Then, the 45 nm thick blend layers (denoted as T/FG-BL) with TIPS-Pen distributing in the matrix of PS dielectric were quickly spin-coated on the surface of the P(NDSI2OD-T2) film from their blend solutions in chlorobenzene. Here, the TIPS-Pen and PS acted as the floating-gate and tunneling layer, respectively. The designed mass ratios of 9:1, 3:7, 5:5, and 1:3 for PS versus TIPS-Pen, respectively, were used to investigate

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the influence of the content of TIPS-Pen in the T/FG-BL on the memory performances. Then, a 320 nm thick PMMA was spin-coated on the surfaces of T/FG-BL films as the blocking layer from its 2-ethoxyethanol (2E) solution. These three layers were annealed at 110 °C in sequence for 10, 10, and 120 min to remove the residual solvents. After the thermal deposition of 80 nm thick Al gate electrode on the surface of PMMA through a shadow mask, all devices were patterned by oxygen plasma etching to finish the fabrication with the arrayed Al as the blocking mask. The three-dimensional structure schematic of our memory is shown in Fig. 1. All FG-OTFT-NVMs were characterized with a semiconductor parameter analyzer (Keithley 4200 SCS) in the ambient atmosphere at the room temperature. The thicknesses of the semiconductor layer, T/FG-BL and blocking layer were measured using a Dektak 6 Surface Profiler.

The surface morphology of the semiconductor layer and the microstructures of T/FG-BL films were first investigated by atomic force microscopy (AFM) in height and phase contrast because they had an important effect on the performances of the memory devices. The spin-coated polymer P(NDI2OD-T2) semiconductor layer exhibited a uniform and smooth surface morphology with a root mean square (RMS) roughness of 0.651 nm (Fig. 2(a)). Figs. 2(c)–2(f) show the microstructures of the T/FG-BL films consisted of PS and TIPS-Pen at different proportions of 9:1, 7:3, 5:5, and 1:3, respectively. The AFM images demonstrated that all the T/FG-BL films exhibited a uniform morphology. The phase-separation of the PS and TIPS-Pen occurred during the spin-coating. The aggregating TIPS-Pen nano-domains became more obvious with the increasing TIPS-Pen content, especially for the case of PS:TIPS-Pen at the proportion of 1:3 (Fig. 2(f)). The surface roughness of the T/FG-BL films increased with the increasing TIPS-Pen content due to its aggregating. In the T/FG-BL films with a low TIPS-Pen content, the TIPS-Pen nano-domains were distributed in the matrix of PS (Figs. 2(c) and 2(d)), while phase inversion occurred in which PS nano-domains were embedded in the TIPS-Pen matrix (Fig. 2(f)) at the case of high TIPS-Pen content with a PS:TIPS-Pen proportion of 1:3.

Both PS and TIPS-Pen cannot be dissolved in a 2E solvent, which ensured that the spin-coating of PMMA blocking layer did not damage the under formed T/FG-BL films. Although polymer P(NDI2OD-T2) can also be dissolved in chlorobenzene, chlorobenzene is not an orthogonal solvent for P(NDI2OD-T2) and T/FG-BL. The subsequent spin-coating of the T/FG-BL films by minimizing the contact time of chlorobenzene on P(NDI2OD-T2) did not damage the previously formed semiconductor layer, which was demonstrated by the good electron mobility and highly stable

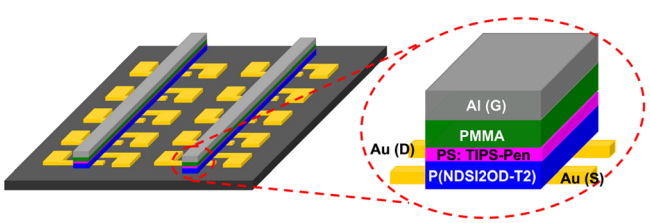

FIG. 1. Schematic diagram of the top-gate FG-OFET-NVMs.

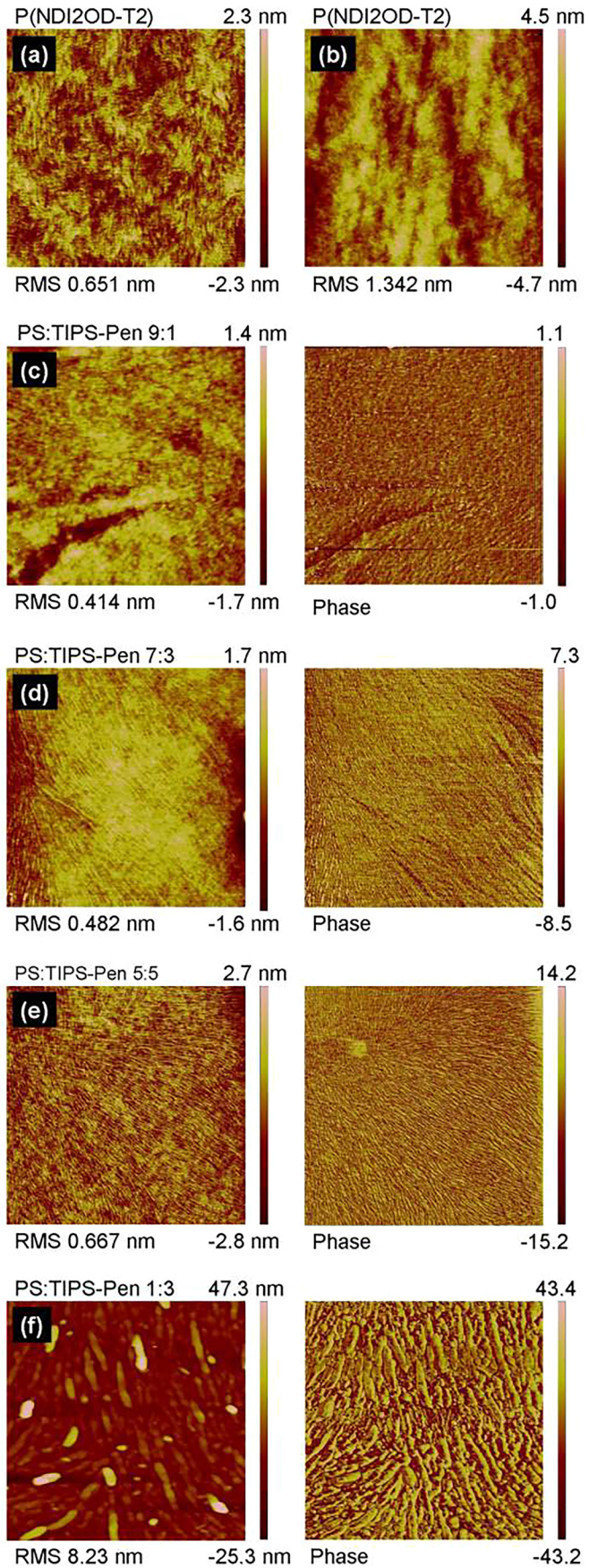

FIG. 2. The AFM images of P(NDI2oD-T2) films (a) on the Si/SiO_2 substrate and (b) on the PES substrate. The AFM images in height and phase contrast of the T/FG-BL films with the proportions of PS:TIPS-Pen at (c) 9:1, (d) 7:3, (e) 5:5, and (f) 1:3 spin-coated on the surface of P(NDI2OD-T2). The area size is 5 μm × 5 μm.

and reliable memory performance in our devices. Our work provides a guiding strategy for solution-processed FG-OTFT-NVMs with a multilayer architecture, in which the solvents for the deposition of upper layer are not required to limit to the orthogonal solvents. Limit to the orthogonal solvents cannot greatly broaden the selection range of the semiconductors and dielectrics to form a flash memory with a multilayer structure by the solution spin-coating method.

The typical electrical transfer characteristics of the FG-OTFT-NVMs with the T/FG-BL films consisted of PS:TIPS-Pen at various proportions of 9:1, 7:3, 5:5, and 1:3 are shown in Fig. 3(a). The transporting mode of typical ambipolar charges was obtained in all transistors, for the drain-source current (I_{DS}) increased with the increase of gate voltage (V_G) in both positive and negative quadrants when the devices operated in the linear region with a drain-source voltage (V_{DS}) of 10 V. In these transistors, electrons were the majority carrier and holes were the minority carriers, demonstrated by the stronger right arm and the weaker left arm in the transfer curves (Fig. 3(a)). The linear mobility (μ_{lin}) of transistors was extracted based on the conventional MOSFET model described as: $I_{DS} = \frac{W}{L}\mu_{lin}C_i(V_G - V_T - \frac{V_{DS}}{2})V_{DS}$, where V_T is the threshold voltage and the C_i is the gate dielectric layer capacitance per unit area. The C_i of the total dielectric layer consisting of bilayer of PMMA and T/FG-BL in series was calculated from the following equation: $1/C_i = 1/C_{PMMA} + 1/C_{T/FG-BL}$, where C_{PMMA} and $C_{T/FG-BL}$ are the capacitance per unit area of the PMMA ($\varepsilon \approx 3.5$) layer and the T/FG-BL, respectively. The calculated $C_{T/FG-BL}$ was in the range of 51–59 nF/cm^2, depending on the composition of PS ($\varepsilon = 2.6$) and TIPS-Pen ($\varepsilon \approx 3.0$). The calculated C_i was of 8.2–8.3 nF/cm^2, rarely depended on the composition of T/FG-BL, due to the low C_{PMMA} of about 9.7 nF/cm^2. The extracted linear electron mobility (μ_e) was 5.0–6.5 $\times 10^{-2}$ cm^2/Vs in all devices, not depending on the proportion of PS and TIPS-Pen. Normally, the charges transport in the first few molecular monolayers of the channel adjacent to the gate dielectric in the organic thin-film transistors (OTFTs).[19] Thus, the interface morphology of the semiconductor/dielectric had a key effect on the carrier mobility in OTFTs.[19] The good electron mobility in our memories suggested that there was a good interface morphology of the P(NDI2OD-T2)/PS.

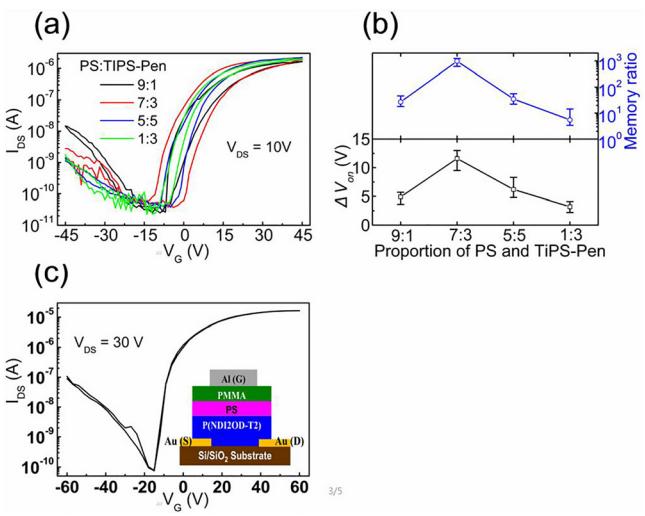

FIG. 3. (a) The linear transfer characteristics of the FG-OTFT-NVMs with the T/FG-BL films consisted of various TIPS-Pen contents. (b) Evolution of the memory ratio and memory window of the devices with the proportion of PS versus TIPS-Pen in the T/FG-BL films. The data were extracted from 10 memory devices on one substrate. (c) The linear transfer characteristics of a control transistor without TIPS-Pen embedded in the PS dielectric. The inset of part c shows the structure diagram of the control transistor.

Obviously, hysteresis characteristics were obtained in all the transistors when the V_G scanned in bi-direction between ±45 V, indicating a promising application as a memory. The memory window (ΔV_{on}) and the memory ratio are two important parameters of a memory. The former is the difference of the turn-on voltage (V_{on}) at Boolean 0 and 1 states. Here, V_{on} was defined as the V_G at which the I_{DS} increased to 1.0 nA. The latter is the ratio of two I_{DS} at Boolean 0 and 1 states, respectively, at a constant reading voltage ($V_R = V_G$). Both the memory window and memory ratio obviously depended on the proportion of PS versus TIPS-Pen, as summarized in Fig. 3(b). The both first increased with the TIPS-Pen content increasing from 10% to 30% in the T/FG-BL and then decreased with the further increase in the TIPS-Pen content. In general, the ΔV_{on} is proportional to the density of the charges trapped in the floating-gate.[12] In the present transistor memories, the nano-domain distributing TIPS-Pen acted as the charge trapping sites, demonstrating that no hysteresis characteristic was observed in a control transistor without TIPS-Pen molecules embedded in the PS dielectric, as shown in Fig. 3(c). The density of the charge trapping sites increased with the increase in the TIPS-Pen content in the matrix of PS at low content, which resulted in an increasing ΔV_{on}. However, the further increase in the TIPS-Pen content resulted in the enlarging of the TIPS-Pen nano-domain size and the decreasing in the density of the charge trapping sites due to the obvious aggregation of TIPS-Pen (Figs. 2(e) and 2(f)). In the case of the PS:TIPS-Pen proportion at 1:3, the charge transfer between P(NDI2OD-T2) and TIPS-Pen resulted in a relative small hysteresis loop. The similar evolution of the memory ratio at the V_R of 0 V with the proportion of PS versus TIPS-Pen was obtained, due to the modulation effect of the trapped charges on the I_{DS}. The above results indicated that the optimal memory window and memory ratio were achieved at a transistor memory with a T/FG-BL consisted of PS and TIPS-Pen at a proportion of 7:3.

To further prove the memory performance, the V_P/V_E pulses of ±55 V were supplied to switch the 0 and 1 states, respectively, in the memory with an optimal T/FG-BL consisted of PS and TIPS-Pen at a proportion of 7:3. During the supplying V_P/V_E pulses for 5 ms, the V_{DS} was always maintained short circuit. In the initial transfer curve measured before the supplying of V_P/V_E, a V_{on} near to 0 V was observed in the memory, as shown in Fig. 4(a). By supplying a V_P of −55 V, the transfer curve negatively shifted due to many holes that were injected and trapped in the floating-gate from the channel. As a result, a negative V_{on} of −13.5 V was obtained (Fig. 4(a)), denoting as 1 state. By supplying a V_E of 55 V, the transfer curve shifted to be more positive than that at the initial state, due to many electrons that were injected into the floating-gate from the channel, which overwrote the previous trapped holes. As a result, a positive V_{on}

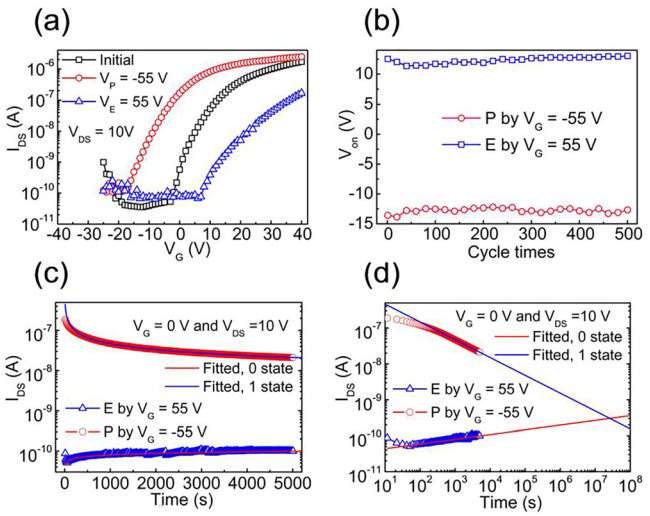

FIG. 4. (a) Transfer characteristics measured in sequence of the initial, P and E states and (b) switching endurance property the memory device. The retention properties of the experiment data and the fitted results in the memory device are shown by a (c) linear and (d) exponential time coordinate, respectively. In the present memory device, the T/FG-BL film consisted of PS and TIPS-Pen at a proportion of 7:3.

of 13.0 V was obtained (Fig. 4(a)), denoting as 0 state. Thus, a ΔV_{on} of 26.5 V was achieved at the supplied V_P/V_E of ±55 V. Then, the values of V_{on} were repeatedly switched between 1 and 0 states, owing to both holes and electrons that were injected into the floating-gate from the channel that overwrote each other at the supplied cyclic V_P/V_E. The V_{on} at both 1 and 0 states maintained well and approximated to their initial values with the switching operations up to 500 cycles, as shown in Fig. 4(b), indicating a high reliable switching endurance property.

Benefited from the large negative and positive V_{on} at the 1 and 0 states, respectively, the V_R could be defined at V_G of 0 V, which is considered as an optimizing condition for the reading operation of memory devices due to the lowest power consumption and the weakest external influence. As a result, the memory ratio of about 2000 was achieved at V_R of 0 V in the present optimal memory (Fig. 4(a)). To investigate the stability of the data storage in the present molecular floating-gate memory, we measured the retention characteristics with the reading current (I_{DS-1} and I_{DS-0}) at both 1 and 0 states as the function of time at V_R of 0 V and V_{DS} of 10 V after programming (P) and erasing (E) operations at the supplied V_P/V_E of ±55 V, respectively, as shown in Figs. 4(c) and 4(d). During the measuring time range of 5000 s, the reading I_{DS-1} and I_{DS-0} had a slightly degradation. Both the relations of the I_{DS-1} and I_{DS-0} with time were well fitted by linear functions in the double-log scale,[20] as shown in Figure 4(d). The fitted results indicated that the present memory had a long retention time up to 10^7 s.

Furthermore, the flexible FG-OTFT-NVM with an optimal T/FG-BL consisting of PS and TIPS-Pen at the proportions of 7:3 was fabricated on the poly(ether sulfone) (PES) substrate at the same conditions. A good nonvolatile memory was also obtained with a large ΔV_{on} of 20 V, memory ratio of about 5000 at V_R of 10 V, and long charge storage retention ability up to 10^7 s, as shown in Figs. 5(a) and 5(b). However, the spin-coated P(NDI2OD-T2) semiconductor

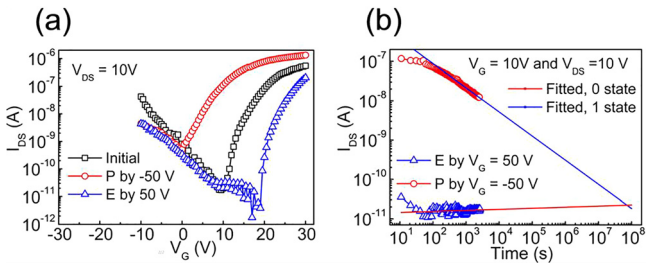

FIG. 5. Transfer characteristics measured in sequence of the initial, P and E states and (b) the retention properties of the experiment data and the fitted results in a flexible memory device on the PES substrate, with the T/FG-BL film consisted of PS and TIPS-Pen at a proportion of 7:3.

film on the PES substrate exhibited a relative rough morphology (Fig. 2(b)), which induced many charges to be trapped at the interface of PES/P(NDI2OD-T2). These trapped charges resulted in the relative positive V_{on} at the initial, 1 and 0 states, respectively, as shown in Fig. 5(a). Thus, the V_R was chosen at 10 V rather than 0 V, for well distinguishing the reading current at binary 1 and 0 states.

In conclusion, we have fabricated FG-OTFT-NVMs with its multilayer core architecture processed by a fully solution spin-coating method. By selecting a proper proportion of TIPS-Pen versus PS acting as the floating-gate and tunneling layer, respectively, an optimal memory was achieved, with a memory window larger than 25 V, reliable switching endurance property over 500 cycles and a stable charge storage retention longer than 5000 s with a memory ratio larger than 10^2.

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