On-chip Optical Sense Strategy Illustrated in the Case of Flash Memory System

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Abstract**—**We proposed and demonstrated a novel scheme for simultaneous optical sense electric memory cell states aiming to enhance the data-reading speed showing significant improvement. For the traditional electrical read-out method, it is impossible to simultaneously sense the information from more than two memory cells on the same bit-line (BL). However, with photonics, different wavelengths do not interfere. Therefore, by converting each memory information into different optical wavelength signals, and multiplexing them (for all bit states) into a single optical waveguide, we can simultaneously sense all memory information and transmit them optically. Experimentally, we demonstrated SONOS (silicon-oxide-nitride-oxide-silicon) transistor as the memory cell, monolithically integrated with optical sense circuits (microring resonator, MRR). Results show that the effective reading speed can be enhanced by 1200 times with 100 nm spectrum ranges.

I. Introduction

Memory products are used in many applications, and are growing at an alarming rate. With the ever increasing memory capacity, how to increase the memory-reading bandwidth becomes challenging for a system with a large quantity of data. For high speed and low power consumption, optical interconnect in lieu of electrical interconnect becomes the development trend in terms of future data communication system [1]. How to link optical interconnect into electronic memory to improve the performance can be a rewarding topic. Even though several existing works are trying to do so [2-3], but memory reading is still done electrically. It does not overcome the slow electrical reading speed issue. Recently, we had proposed and demonstrated electrically programmable optical memory circuits [4], but it is with higher operation voltage (~20 V). Here, we propose a novel optoelectronic integration circuit (OEIC) for optical sense and transmit flash memory array information. Each flash memory correspondingly controls MRR's oscillation wavelength. The memory information can be sensed by the optical signal with a significantly increased reading speed.

II. Principle and Designation

The topological schematic graph of general electrical memory array is shown in **Fig. 1(a)** and the reading process chart is as in **Fig. 1(b)**, in which, on the same bit line, memory cells can be sensed only one at a time. **Figure 2** illustrates the operating principle of the proposed optical sensing scheme. For a given memory array, each memory cell is integrated to control an MRR; such an MRR is designed to oscillate with different wavelengths (λ_0~λ_N) and integrated with P-i-N junction waveguide (**Fig. 2(a)**). The junction is connected with an electrical memory cell. When the memory cell is programmed to ON/OFF state, the current through MRR P-i-N junction waveguide is in ON/OFF state. Thus, each MRR's oscillation wavelength is with/without a shift. A wideband light source transmits in shared bus waveguide. It will record all MRR oscillation wavelengths in the spectrum, i.e. record all memory cell information into optical signals. In the receiving end, the optical information can be de-multiplexed, and converted back to the electrical signal by a photodetector array (**Fig. 2(b)** [5]). Correspondingly, the reading sequence chart is presented in **Fig. 2(c)**. At a time, information from N+1 memory cells can be read. N+1 is equal to the optical channel numbers that are the light bandwidths dividing the channel space. Thus, there is N+1 times improvement than in the conventional electrical read-out method. Another advantage is that all the optical information between the transmitter and receiver can be directly linked by the fiber. It is in line with the development trend of light replacing copper in the interconnect. **Fig. 3** explains a SONOS transistor, as memory cell for an example, to control the MRR oscillation wavelength in detail. **Fig. 3(a)** is a tilt-view showing the MRR and SONOS memory cell structure. MRR's ridge waveguide is with P-i-N junction. P-type slab is a drain electrode and N-type slab is a shared electrode of SONOS transistor. **Fig. 3(b)** is the schematic of SONOS cross-section with MRR ridge waveguide and their equivalent circuit. When the SONOS transistor is at ON- or OFF-state, the drain current is significantly different, which subsequently results in different carrier densities in the P-i-N junction, thus shifting the MRR's peak-resonating wavelength ($\Delta\lambda$) (**Fig. 3(c)**). The table provides the equations describing the relationship of $\Delta\lambda$, optical power changes as functions of various parameters.

III. Fabrication Process

We fabricated the devices on an 8-in SOI wafer by standard CMOS-compatible processes in the Institute of Microelectronics (IME), Singapore. The SOI wafer is 340 nm top crystalline silicon with 2 μm BOX. First, deposit SiO_2/SiN as a hard mask to partially etch 240 nm Si to form bus waveguide and MRR. Then, coat the photoresist (PR) to cover the MRR area, and etch the remaining 100 nm Si to the

BOX. Thus, the MRR and bus waveguide are ridge- and channel-waveguide, respectively. Flowing is twice the implantation to form a uniform distribution P-well. The dose and energy of boron ion are 1×10^{13} cm^{-2}, 20 keV and 5×10^{12} cm^{-2}, 12 keV. After clearing wafer, deposit 300 nm SiO_2 and etch back to create the spacer for protection-waveguide sidewall. Then, thermally grow 2.5 nm SiO_2, deposit 3.4 nm SiN, 5.5 nm SiO_2, and 100 nm a-Si by LPCVD. The wafer is blankly implanted phosphorous with the dose of 4×10^{15} cm^{-2}, and energy of 35 keV. After PR coating, transfer control-gate patterns into PR. Etch the a-Si/ONO stack layers. After wafer cleaning, deposit 10 nm SiO_2 and 100 nm SiN by LPCVD. SiN is etching back as spacer of the gate. Do PR coating and transfer the drain electrode ohmic contact pattern into PR. Implant boron with a dose of 4×10^{15} cm^{-2} and energy of 10 keV. A similar process is used to implant phosphorous with the same dose, but with an energy of 27 keV for the control gate and source ohmic contact. The next process is to deposit SiO_2 and open contact window, deposit AlSiCu, and form the electrode. Figure 4 shows the image of the device. **Figure 4(a)** is the top-view picture of an optical microscope. The MRR is with wide 500 nm ridge waveguide and 15 μm radius. The gap between the MRR and bus waveguide is 300 nm. In **Fig. 4(b)**, SEM indicates the connection portion of SONOS and MRR. In SONOS transistor, the channel width is 3 μm and length is 200 nm. **Fig. 4(c)** displays the cross-sectional view of SONOS. The P- and N-type Si are colored in purple and blue, respectively. The thickness of the P-well and control gate is 100 nm. The slab thickness is ~64 nm. The ONO stack layers between the P-wall and control gate are zooming in **Fig. 4(d)**. They are 2.5 nm/3.4 nm/5.5 nm, respectively.

IV. RESULS & DISCUSSION

First, we test the static characteristics of the SONOS transistor, from which the operating points can be determined. **Fig. 5(a)** shows the ON/OFF states of drain current (top) and current difference (bottom) as a function of V_{GS} with V_{DS} =1.5 V. The gate voltage sweeps from -10 V to 10 V and drops back. To make the current difference between ON/OFF states as much as possible, we chose the control gate voltage as the threshold of OFF state. **Fig. 5(b)** shows the linear- and log-plots of drain current via gate voltage. The threshold voltages for ON/OFF states are -2.82 V and 0.35 V, respectively. Thus, the threshold voltage (V_t) window is ~3.17 V. Wider window will give the device a higher stability. **Fig. 5(c)** shows the source/drain I-V curves vs. V_{DS} with different V_{GS}. In the left figure, the lines from bottom to top represent the gate voltage increasing from 0 V to 10 V with steps of 1 V. In the right figure, the lines from top to bottom represent the gate voltage from 10 V to 0 V with a step of -1 V. **Figures 6 and 7** show the optical response of the corresponding MRRs. **Fig. 6** shows the optical spectrum from bus waveguide with FSR (free spectral region) of 6 nm (top), and zoom-in resonance at λ=1499.72 nm with full-width at half-maximum (FWHM) ~40 pm (bottom). Thus, the Q-value is ~37500. The narrower the FWHM, the better will be the resolution of the states. **Fig. 7** indicates the MRR spectra (top), and wavelength shift value (bottom) with drain currents. It is a clear indication that the resonating wavelength is blue-shifted with increasing drain current. When the current is larger than 0.7 mA, the resonating wavelength shows a red shift. This indicates that the thermal effect begins to dominate. **Fig. 8** shows the experimental implementation of an optical sense method. For ON/OFF state at V_{GS} =0, the drain current difference is ~170 μA (showing inset figure), and the resonating wavelength shift is ~114 pm. Assuming that the carrier wavelength is set at the original wavelength, the extinction ratio of 19.8 dB is achieved. In fact, the wavelength shift of an FWHM (40 pm) is sufficient to distinguish the ON/OFF states. Thus, with a channel spacing of double FWHM (80 pm), there can be 75 channels packed within a 6 nm of FSR, corresponding to a 75 times enhancement in the effective reading speed when compared with the conventional electronic method. For the sake of an argument, it can be further enhanced with ~1200 times if using, e.g., LED light, with 100 nm broad spectrum ranges and split into 16 slices. **Fig. 9** shows the implementation of a mini-type system of optically sensed SONOS memory cell array. **Fig. 9(a)** is the optical micrograph (top) and spectra (bottom) of the OEIC integrating four MRRs with different radii coupled to a single bus waveguide. **Fig. 9(b)** shows the measured ON/OFF state spectra around each MRR oscillation range. The ON/OFF extinction ratios are 22.0 dB, 10.4 dB, 14.1 dB, and 20.0 dB, respectively. **Fig. 10** shows the dynamic spectrum and optical response time. The rise- and fall-time are 5 ns and 3 ns, respectively

For all-pass MRR, the oscillation optical states lie at low optical intensity. By using add-drop (AD) MRR, the ON/OFF states could be right on high optical power. **Fig. 11** shows the linear- and log-plots of the drain current vs. gate voltage under different drain biases for AD-MRR with dual SONOS memory cells. The bias of drain is increased from 1 V to 1.5 V by a step of 0.1 V. The threshold voltage window width is ~1.5 V. **Fig. 12** shows the spectrum at ON/OFF states with a wavelength shift of 121 pm. AD-MRR makes the optical reading circuit more flexible. The oscillation wavelength shifts 121 pm @ V_{GS}=0. Optical extinction ratio is 14.1 dB. Inset: the operation points on I_D -V_{GS} curve.

V. SUMMARY

We proposed an optical sense memory system. Using CMOS technology, we demonstrated a system that integrates SONOS transistor memories and MRR's optical sensing circuit. Up to 1200 enhancements of the reading speed are demonstrated experimentally.

ACKNOWLEDGMENT

The first author is grateful for the support from the program of National Natural Science Foundation of China (NSFC) under Grant Nos. 61177090 and 61377048.

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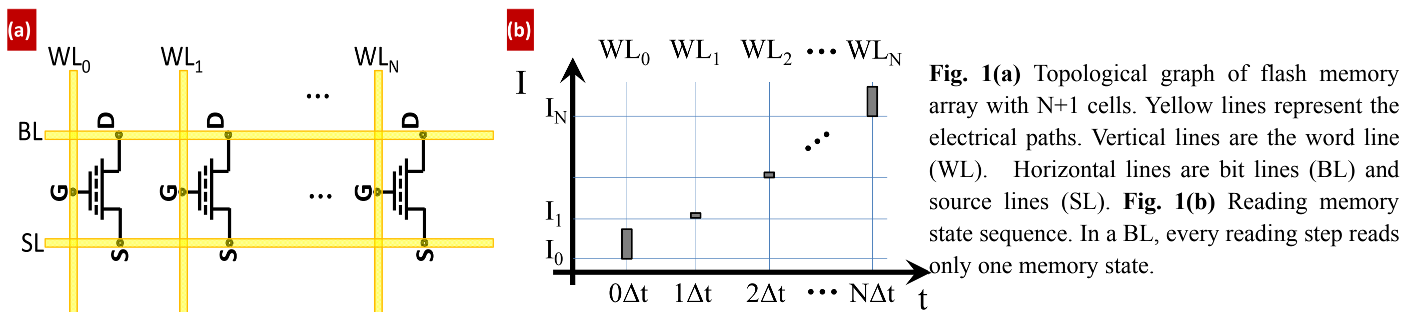

Fig. 1(a) Topological graph of flash memory array with N+1 cells. Yellow lines represent the electrical paths. Vertical lines are the word line (WL). Horizontal lines are bit lines (BL) and source lines (SL). **Fig. 1(b)** Reading memory state sequence. In a BL, every reading step reads only one memory state.

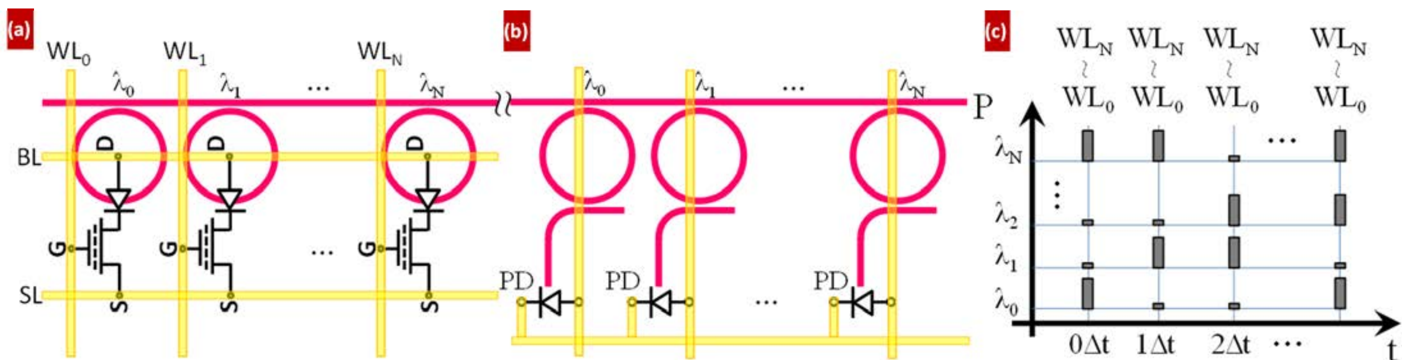

Fig. 2(a) The proposed optical read-out flash memory array. Red and yellow lines represent optical waveguides and metal lines, respectively. All the drain terminals of flash memory are connected with MRRs. **(b)** Illustrator of WDM receiver. The optical signals are de-multiplexed and converted to electrical signal by individual photodetector. **(c)** Optically read-out memory state sequence. Each step can simultaneously read out all the N+1 memory cells information. The reading speed is N+1 times enhanced.

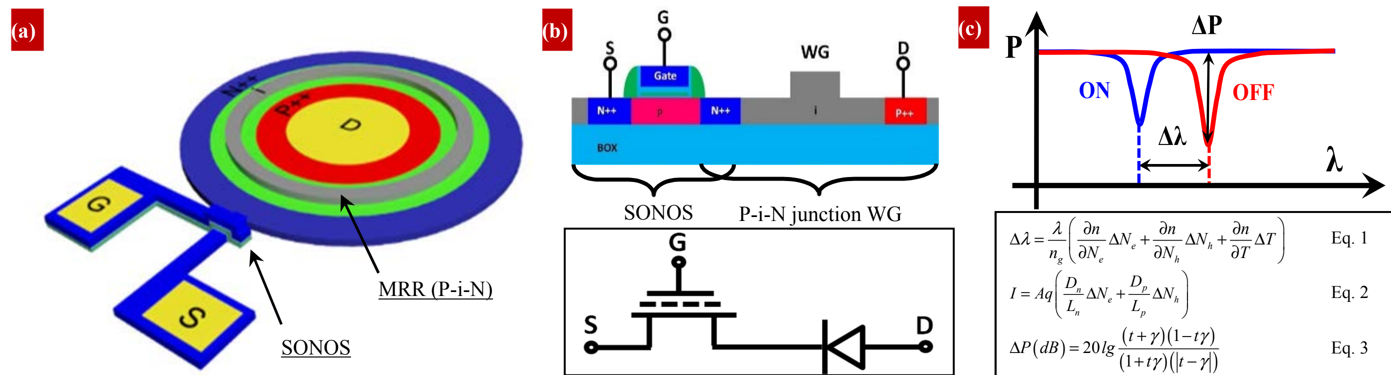

Fig. 3 (a) Schematic of SONOS flash memory integrated MRR. **(b)** Cross-sectional schematics (top). The blue and red regions represent N- and P-type silicon. The MRR ridge waveguide is laterally integrated with P-i-N junction. The N++ is shared with SONOS flash memory. Bottom is an equivalent circuit of the SONOS integrated MRR. **(c)** MRR spectra with ON (blue) /OFF (red) states of SONOS memory (top). Bottom equations describe the relationships between wavelength shifts, drain current, and power density.

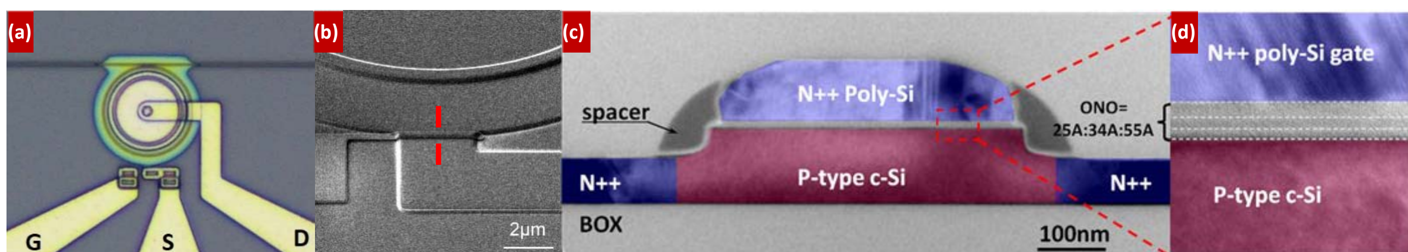

Fig. 4 (a) Microscope image of MRR integrated with SONOS memory cell. The radius of MRR is 15 μm. **(b)** SEM of MRR and SONOS memory cell. In SONOS memory cell, the channel width is 3 μm, length is 200 nm. **(c)** The cross-sectional TEM of SONOS along the dashed red color line in **(b)**. P-type well is boron doped with an implantation density of 10^{13} cm^{-2}. Source, drain and control gate are phosphorous doped with an implantation density of 4×10^{15} cm^{-2}. **(d)** The zoom-in TEM of the ONO structure. From bottom to top, the thicknesses are 25A, 34A and 55A, respectively.

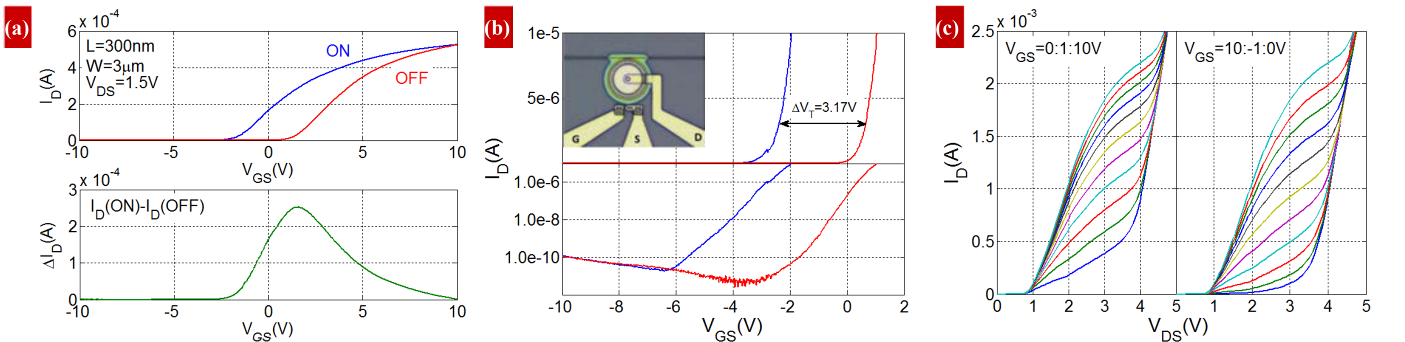

Fig. 5 (a) ON/OFF drain current (top), and current difference (bottom) vs. gate voltage. The length and width of the channel are 300 nm and 3 μm, respectively. The source/drain voltage is fixed at 1.5 V. **(b)** The linear (top) and logarithmic (bottom) plots of source/drain current vs. gate voltage. **(c)** The source/drain I-V curve at different gate biases. In the left figure, the lines from bottom to top represent the gate voltage increasing from 0 V to 10 V with a step of 1 V. In the right figure, the line from top to bottom represent the gate voltage from 10 V to 0 V with a step of -1 V.

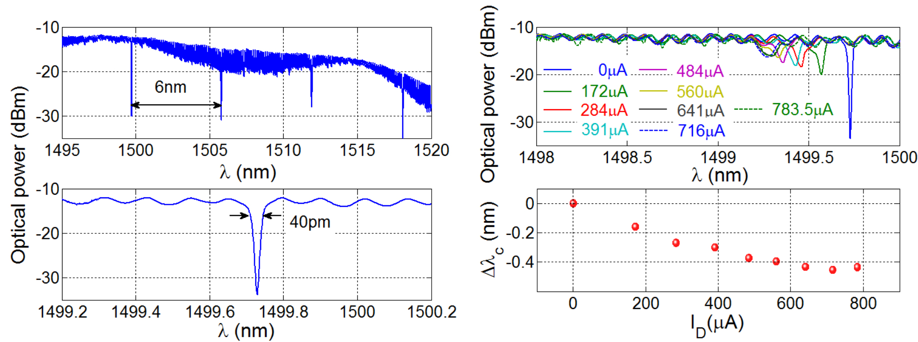

Fig. 6 MRR spectrum (top). The radius of MRR is 15 μm. The FSR is 6 nm. The zoom-in view of the first resonance (bottom).

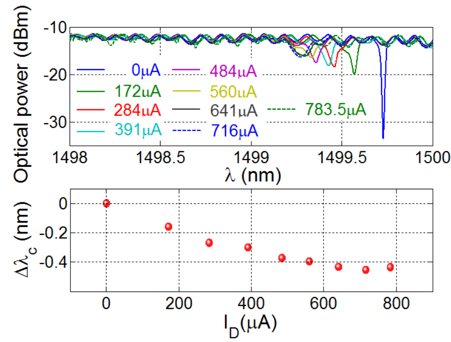

Fig. 7 The spectra of MRR with different drain currents (top), and the oscillation wavelength shift with the drain current (bottom).

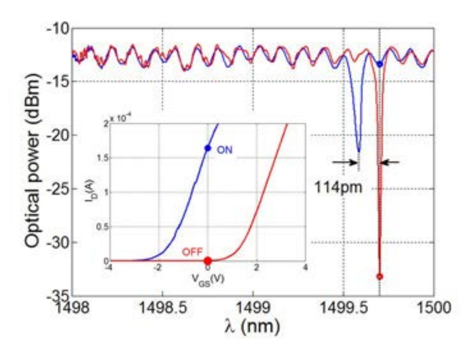

Fig. 8 The spectra of ON/OFF states. The oscillation wavelength blue-shifts 114 pm @ V_{GS}=0. Optical extinction ratio is 19.8 dB. Inset: the operation points on I_D-V_{GS} curve.

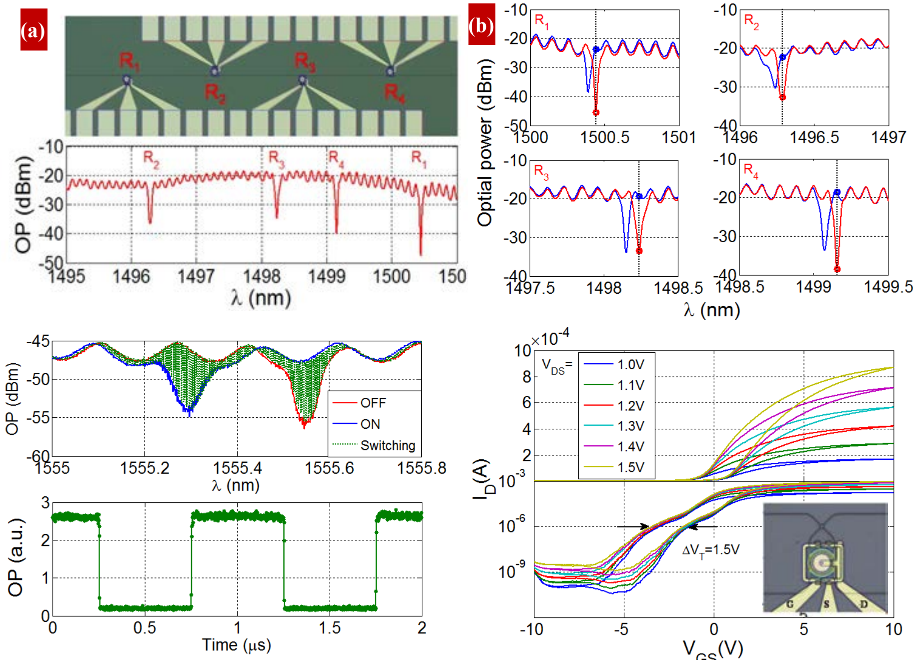

Fig. 9 (a) Microscope image (top) and spectrum (bottom) of a multiplex optical read-out memory system with four MRR/SONOS arrays coupled with a bus waveguide. The radii of the four MRRs increase from 15 μm with a step of 20 nm. **(b)** The spectra showing ON/OFF states for four MRR/SONOS cells. The ON/OFF extinction ratios are 22.0 dB, 10.4 dB, 14.1 dB and 20.0 dB, respectively.

Fig. 10 Fix the V_{GS}=0, and put on a 1 MHz square wave voltage on the V_{DS}. The spectrum is on top and time response is at the bottom. The rise time and fall time are 5 ns and 3 ns respectively.

Fig. 11 Drain current vs. gate voltage with different biases on the drain for AD-MRR. The top and bottom figures are linear and logarithmic plots. The bias of drain is increased from 1 V to 1.5 V by a step of 0.1 V.

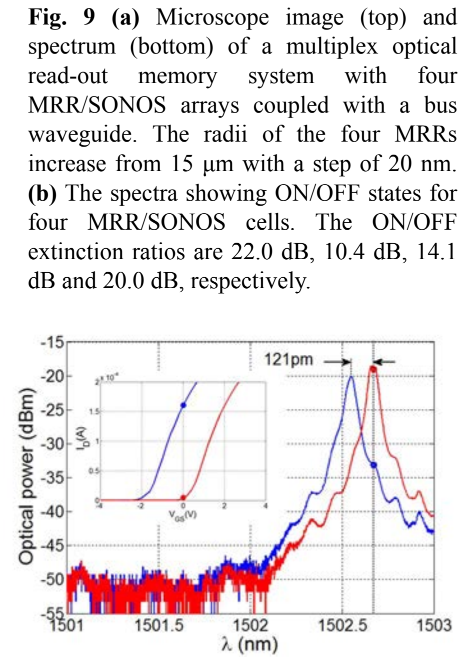

Fig. 12. The spectra at on/off states. Blue line and red line denote ON/OFF states, respectively. The oscillation wavelength shifts 121 pm @ V_{GS}=0. Optical extinction ratio is 14.1 dB. Inset: the operation points on I_D-V_{GS} curve.