Research Article | Vol. 24, No. 19 | 19 Sep 2016 | OPTICS EXPRESS 21744

Optics EXPRESS

Silicon photonic integrated circuits with electrically programmable non-volatile memory functions

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Abstract: Conventional silicon photonic integrated circuits do not normally possess memory functions, which require on-chip power in order to maintain circuit states in tuned or field-configured switching routes. In this context, we present an electrically programmable add/drop microring resonator with a wavelength shift of 426 pm between the ON/OFF states. Electrical pulses are used to control the choice of the state. Our experimental results show a wavelength shift of 2.8 pm/ms and a light intensity variation of ~0.12 dB/ms for a fixed wavelength in the OFF state. Theoretically, our device can accommodate up to 65 states of multi-level memory functions. Such memory functions can be integrated into wavelength division mutiplexing (WDM) filters and applied to optical routers and computing architectures fulfilling large data downloading demands.

OCIS codes: (250.3140) Integrated optoelectronic circuits; (250.6715) Switching; (130.3120) Integrated optics devices; (130.4815) Optical switching devices; (130.2790) Guided waves; (210.4680) Optical memories.

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#270155 http://dx.doi.org/10.1364/OE.24.021744
Journal © 2016 Received 8 Jul 2016; revised 23 Aug 2016; accepted 24 Aug 2016; published 9 Sep 2016
Corrected 12 September 2016

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1. Introduction

Silicon photonics technology has recently been utilized to leverage integrated optics and CMOS fabrication platforms to build integrated optoelectronic circuits on silicon substrates. This technology has begun to play an increasingly important role in optical communications and optical interconnect applications [1–3]. The development of fundamental devices such as optical switches [4–7], silicon modulators [8, 9], and germanium photodetectors [10, 11] for application in optoelectronics sub-systems such as optical routers, reconfigurable optical add-drop multiplexers (ROADMs), and wavelength selective switches (WSSs) [12–16] promise greater commercialization in the deployment of this technology.

Optical switches form one of the most fundamental components in optoelectronics sub-systems. Light propagation in optical switches can be routed through different paths by applying an electrical bias to the switcher(s). A low switching power is required for reducing on-chip energy consumption, and the most desired feature of such a device is the memory function, so that the configured optical switch states can be retained without large power consumption or no standby power at all. In this context, for the first time to the best of our knowledge, we recently designed and demonstrated a non-volatile electrically programmable photonics memory cell (PMC) employing an all-pass microring resonator structure, which exhibited multi-level memory properties [17]. This device shows potential application in memory reading systems, improving computer memory reading speeds, and partly eliminating von Neumann's bottleneck [18].

In this work, we integrate an add/drop microring resonator (MRR) into an optical switch circuit with multi-level memory functionality. In comparison with a 1 × 1 all-pass MRR, the 2 × 2 add/drop MRR is more suitable for application to optical switches, routers, ROADMs, WSSs, etc. Further, we investigate how electronic pulses can be used to control the memory levels. This feature, combined with optical reading circuits, can be applied in computer

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memory systems to overcome the von Neumann bottleneck issue. We investigate the WDM demultiplexer as an example of an add/drop MRR application. In our demonstrated waveguide memory function, it can be applied as a fine-tuning feature to eliminate fabrication errors induced wavelength drifts while ensuring very low power consumption.

2. Working principles

Figure 1 shows the proposed PMC with programmable and erasable memory functions. The device utilizes a floating gate (FG) transistor structure with the source and drain separated from each other as shown in the figure. The left-hand-side box indicated by dashed lines in Fig. 1 shows a capacitor like optical waveguide with a polycrystalline-silicon (poly-Si) FG separated by a thin oxide dielectric from the crystalline-silicon (c-Si) that connected to the drain (D). On the source side (right-hand-side box with dashed lines), a poly-Si control gate (CG) is positioned above the FG with an oxide-nitride-oxide (ONO) dielectric stack separating the two gates.

The PMC operation principle for programming (write function) is as follows. When a sufficient bias is applied to the control gate (CG) to ensure that the electric field between the electrical source (S) and CG is sufficiently high, source electrons can tunnel through the thin oxide dielectric into the FG. Thereafter, electrons are driven by the self-generated electrical field of the p–n junction and are distributed in the FG, and are subsequently transferred to the drain (D) side. The presence of these injected electrons changes the refractive index of the optical waveguide (labeled as the "ON" state in this work). For the erase operation, the CG voltage is set to 0 V, and the drain terminal is biased with a sufficiently high voltage for electrons to tunnel across the oxide layer between the FG and waveguide (at the drain). This again changes the refractive index of the FG, and turns the device to its "OFF" state.

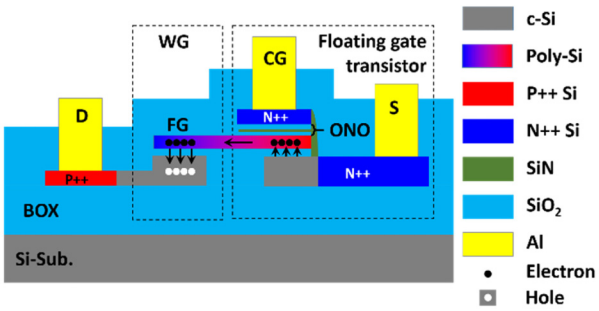

Fig. 1. Cross-section illustration of optical waveguide structure used in our study. WG: waveguide. FG: floating gate. CG: control gate. S: source. D: drain.

3. Fabrication process

The PMC was fabricated by means of standard CMOS-compatible processes at the Institute of Microelectronics (IME), Singapore. The schematic process flow is illustrated in Fig. 2. The starting substrate was an 8-inch silicon-on-insulator (SOI) wafer with a 160-nm-thick top silicon layer deposited on a 2-μm-thick buried oxide (BOX) layer (Fig. 2(a)). A ridge waveguide with slab thickness of 100 nm was next formed (Fig. 2(b)). Plasma-enhanced chemical vapor deposition (PECVD) was used to deposit an oxide layer, and the wafer was planarized to ensure that the silicon waveguide was exposed (Fig. 2(c)). Subsequently, thermal oxidation was performed to form an 8-nm gate oxide. Next, 100-nm poly-Si was deposited by low-pressure CVD (LPCVD), followed by phosphorus (3×10^{12} cm^{-2}, 35 keV) and boron (6×10^{12} cm^{-2}, 13 keV) implantations to form a p-n junction in the FG; the blue and red colors denote n- and p-type regions, respectively (Fig. 2(d)). A film stack of 6-nm TEOS oxide, 3.5-nm LPCVD Si_3N_4, and 6-nm TEOS oxide was deposited to form the ONO layers. Another 100-nm-thick poly-Si layer was deposited by LPCVD to form the CG (Fig.

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2(e)). These stacked layers were etched for source contact doping (Fig. 2(f)). A SiO_2/SiN spacer was formed to protect the FG sidewall before phosphorus implantation (4×10^{15} cm^{-2}, 35 keV) to form the source and CG ohmic contacts (Fig. 2(g)). After etching of the FG and drain (Fig. 2(h) and Fig. 2(i)), boron implantation (5×10^{14} cm^{-2}, 13 keV) was conducted to form the drain (Fig. 2(j)). After dopant activation, SiO_2 deposition (Fig. 2(k)) and two-AlSiCu-layer metallization were performed to complete the device fabrication (Fig. 2(l)).

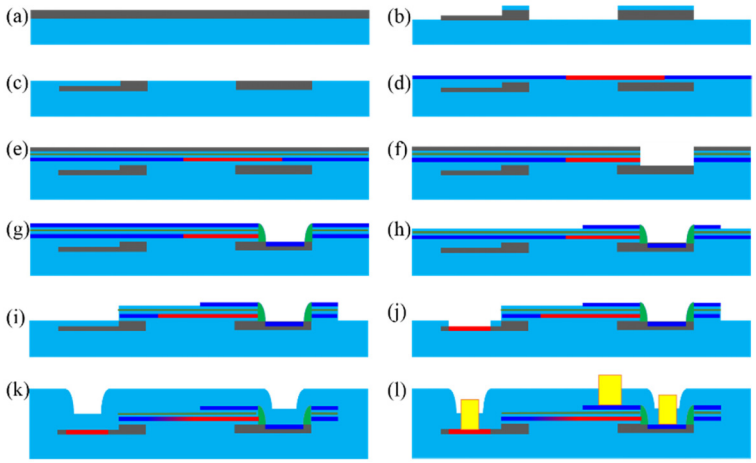

Fig. 2. (a) Silicon-on-insulator (SOI) wafer with 160-nm-thick silicon deposited on 2-μm-thick buried oxide (BOX). (b) Etching of silicon ridge waveguide with hard mask. (c) Deposition of oxide and chemical mechanical polishing (CMP). (d) Deposition of 8-nm thermal oxide and 100-nm poly-Si through low-pressure chemical vapor deposition (LPCVD). (e) Deposition of oxide-nitride-oxide (ONO) and 100-nm poly-Si through LPCVD. (f) Fabrication of open source contact window. (g) Deposition of SiO_2/SiN spacer. (h) Formation of control gate. (i) Formation of floating gate. (j) Opening of drain window and implantation. (k) Fabrication of SiO_2 cladding. (l) Waveguide structure with first metal layer.

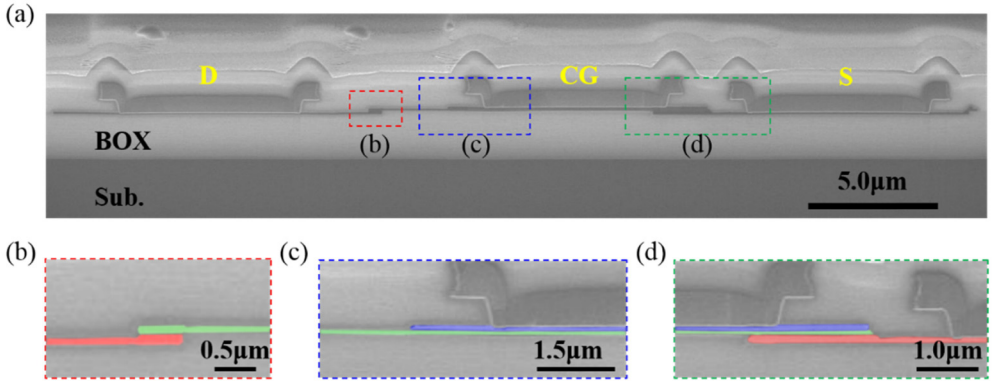

Fig. 3. (a) Scanning electron microscope (SEM) image of photonics memory waveguide. (b) Magnified image of poly-Si/gate oxide/c-Si waveguide. (c) Magnified image of poly-Si/ONO/poly-Si structure. (d) Magnified image of poly-Si/ONO/poly-Si/gate oxide/c-Si structure. Crystalline silicon (c-Si), poly-Si floating gate, and poly-Si control gate are indicated by light red, light yellow, and light blue colors, respectively.

Figure 3 shows the cross-section of the fabricated waveguide structure. Figure 3(a) depicts the scanning electron microscope (SEM) image of the waveguide cross section. Figures 3(b)-3(d) show the magnified images of the waveguide, CG, and stack layers, respectively.

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4. Results and discussion

With the use of the cutback method to extract the waveguide propagation loss performance, we measured the loss to be 2.6 dB/cm for our waveguide with channel dimensions of 500 nm × 160 nm. The capacitor-like waveguide in Fig. 1, the losses of ON (electrons stored in FG) and OFF (electrons tunnel out from FG) states are 5 dB/cm and 1 dB/cm, respectively. In comparison with the add/drop MRR, the all-pass MRR does not provide high extinction ratios (depth of oscillation spectrum profile). To achieve high ratios, the coupling coefficient must be close to the MRR propagation loss [19]. This forms a serious design and fabrication challenge. However, for an add/drop MRR, it is relatively easier to obtain extinction ratios >20 dB for the drop terminal. This property makes the use of this MRR convenient for signal detection. The fabricated add/drop MRR with a radius of 15 μm and the cross waveguide is shown in Fig. 4a. Such kind of crossing-connected MRR structure is widely adopted in such as on-chip optical router and optical matrix switches for on-chip optical interconnection [12, 20]. The gap between the waveguide and the MRR is 200 nm, and the slab thickness is 100 nm. The memory MRR is electrically programmed by sweeping the CG voltage from 0 V to 20 V and back to 0 V. The source and drain are grounded during this operation. The injected electrons in the floating gate are transferred into the MRR waveguide at the drain side. There is a corresponding decrease in the refractive index of the MRR waveguide, resulting in a blue shift of the resonant wavelength (ON state). For the erasing process, the drain voltage is swept from 0 V to 6 V and back to 0 V with a grounded source and control gate. In this case, the MRR resonant wavelength red-shifts due to electron extraction from the floating gate, and this corresponds to the OFF state.

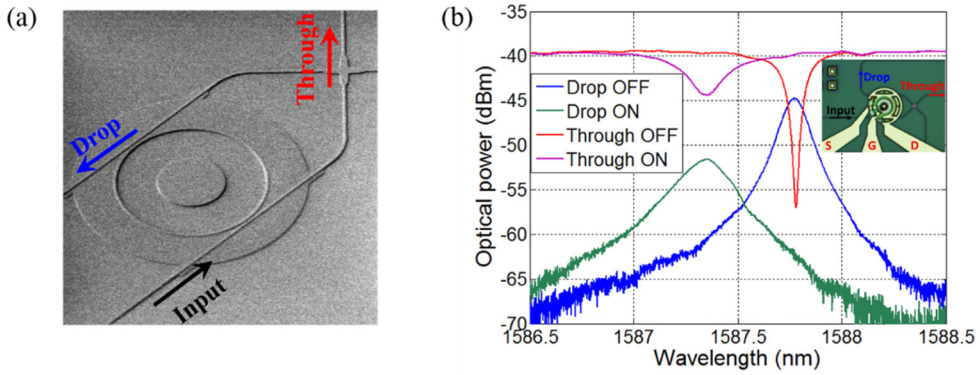

Fig. 4. (a) Scanning electron microscope (SEM) image of add/drop microring resonator memory cell. (b) Through and drop terminal spectra of add/drop microring resonator. Through/drop terminal spectra curves are shown at bottom and top, respectively. The curves are dependent on the electrical voltage pulse width. The optical microscope (OM) image of the add/drop microring resonator device is shown inset.

Figure 4(b) shows the transmission spectra of the ON and OFF memory states; the optical oscillation wavelength is blue-shifted from the OFF state (1587.763 nm) to the ON state (1587.337 nm). The full width half maximum (FWHM) values of the spectra for the OFF and ON states are 130 pm and 293 pm, respectively, and the *Q*-factors corresponding to the OFF and ON states are 12000 and 5400, respectively. If the input light wavelength is fixed at the OFF-state oscillation wavelength (1587.763 nm), for the OFF state, the through- and drop-port power values are −57 dBm and −45 dBm, respectively. The drop direction is ON. For the ON state, the through- and drop- port powers become −40 dBm and −62 dBm, respectively, and the through direction is ON. The memory properties of endurance and retention have been confirmed in our recent work [17], and such add/drop MRR optical switches can be applied in optical routers [12]. Further, the memory function PMC can ensure that the router

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circuit also has a memory function, which can facilitate implementation of circuits with some level of intelligence. The operation voltage can be reduced by reducing the gate oxide thickness. Currently, we use thermal oxidation method to grow 8-nm gate oxide. Alternatively, atomic layer deposition (ALD) can be used in order to grow thinner gate oxide in the order of several angstroms.

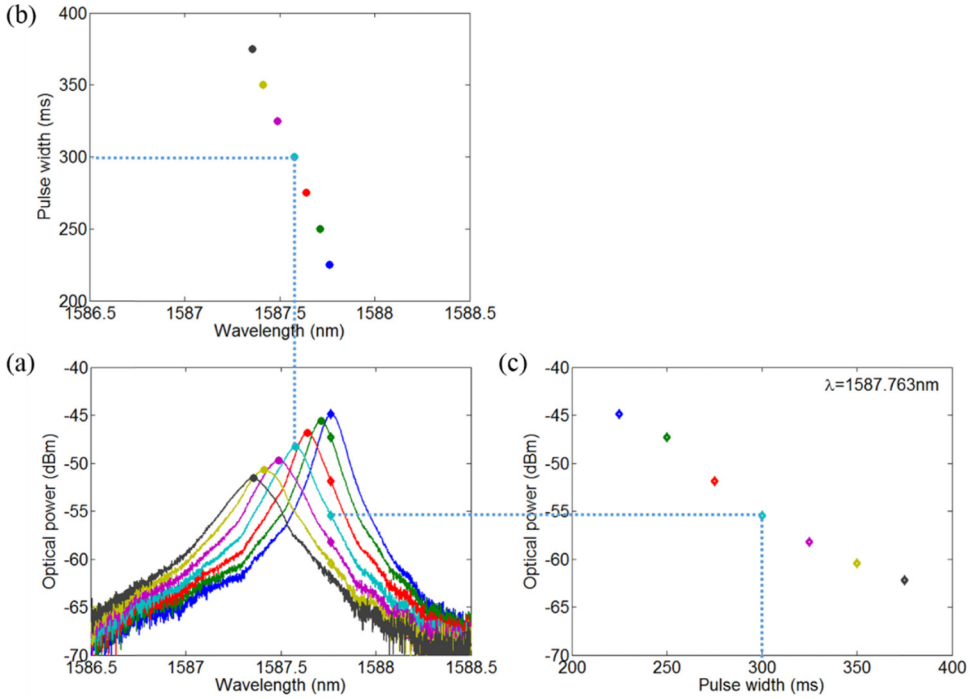

Fig. 5. (a) Drop terminal spectrum with square-pulse-voltage operation. (b) Oscillation wavelength blue-shift with pulse width. (c) Optical power attenuation with pulse width at OFF-state oscillation wavelength.

Figure 5(a) shows the drop spectrum obtained with pulse voltage application. The pulse voltage exhibits a peak voltage of 20 V when the pulse width increases from 225 ms to 375 ms in steps of 25 ms. During the pulse time from 0 to 225 ms, the electrons only charge the capacitor in control gate and source, yet not tunnelling the gate oxide. When the pulse width is larger than 375 ms, the electrons fully fill the floating gate, and increase the voltage of floating gate. The electrons can't tunnel gate oxide and transit to the floating gate. During 225 ms and 375ms, the wavelength shift shows linear property with pulse widths.

There are two primary reasons limiting the PMC with large operation time. First limitation is the electrons tunneling gate oxide mechanism. As the tunneling current is too small, it requires longer time to accumulate enough electrons in order to sufficient index change of the MRR waveguide. The tunneling current can be improved by hot electron injection method [21]. The tradeoff is the increased power consumption. Another reason is the transit time limitation. In order to reduce the optical propagation loss, the distance between the tunneling gate oxide and MRR waveguide is ~10 μm. Thus, the electron transit time under the weak self-built electrical field in the floating gate is long. It can be improved by reducing the device footprint and adding an external electrical field. From Fig. 5(a), we observe that the increasing pulse width causes a blue shift in the spectrum.

Next, we attempt to distinguish the different memory levels from the spectra. We illustrate two methods to realize multiple-level memory functions. The first method involves detection of the wavelength shift. This method is widely applied in label-free biosensor systems [22],

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and it is realized with the use of an electrical read-out from the chip by means of the tracing ring method [23]. This tracing ring method is able to achieve a three-sigma (3σ) of ~0.2-pm wavelength-shift-detection accuracy. Further, the approach is also compatible with complex optical sensor testing platforms [24]. In this study, ON/OFF wavelength shift is 426 pm. In ideal situations, shift levels greater than 2000 are possible. However, in the current testing platform, the MRR oscillation-wavelength testing accuracy is ~6.5 pm. Therefore, the region of ON/OFF wavelength shifts corresponds to more than 65 memory states. Such a large number of memory states, if applied in a mainframe computer with large data-center memory-data readouts, may possibly overcome the so-called von Neumann bottleneck issue [18]. Figure 5(b) shows the oscillation wavelength shift as a function of the pulse width; we observe a fairly linear relationship between the two parameters, with a slope of ~2.8 pm/ms. For an oscillation wavelength shift of 0.2 pm, a pulse width of ~72 μs is required.

The second method to distinguish the memory levels is through optical power detection. This approach uses a fixed input light wavelength for the OFF state oscillation. Figure 5(c) shows the optical power as a function of the pulse width for a fixed wavelength of 1587.763 nm. The pulse width is linearly correlated with the optical power decrease with a slope of ~0.12 dB/ms. Comparing to all-pass MRR structure, such add/drop MRR is more easily to obtain optical response with high extinction ratio from the drop port, which is more suitable for optical power detection method.

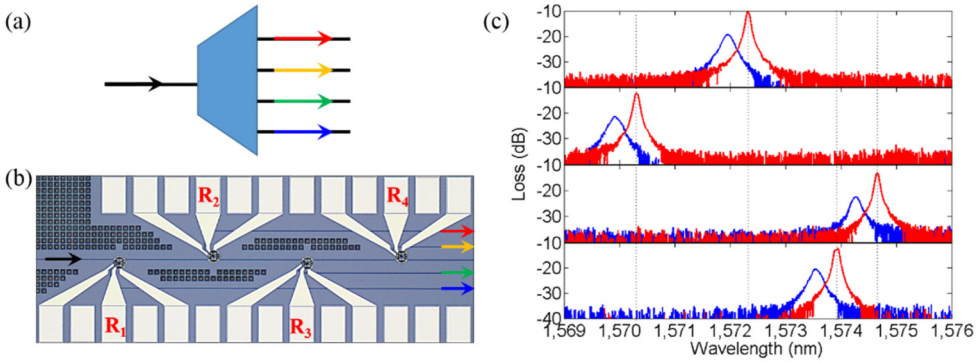

Fig. 6. (a) Schematic of wavelength division multiplexing (WDM) demux. (b) Optical microscope (OM) image of memory functional WDM with 4-channel Add/Drop memory functional MRR integration array. (c) Spectra at drop terminals for ON and OFF states. Red color curves indicate the OFF state and blue color curves indicate the ON state.

We next examine a possible application of our device. Wavelength division multiplexing (WDM) forms a basic component for constructing network-on-chip devices. Figure 6(a) shows the schematic of the WDM demultiplexer (demux) function. The demux splits a composite wavelength signal into separate channels. Conversely, the multiplexer (mux) combines different-wavelength signals into one channel. The mux and demux can be applied to transceivers, WSSs, optical add/drop multiplexers, and ROADMs. However, conventional technology cannot eliminate fabrication errors that cause wavelength drifts. The existence of such a drift requires additional fine-tuning to shift the wavelength to the targeted value. Further, for maintaining the "shifted" wavelength, the circuit will require power to maintain the states of interest. Figure 6(b) shows an example of a 4-channel WDM (de)multiplexer integrated with an MRR PMC. In the study, we used four MRRs (R_1 to R_4 in the figure) with different radii to obtain four unique oscillation wavelengths. Figure 6(c) shows the response spectra of the ON/OFF states in different channels. With this setup, we can control the electrical pulse width, as in Fig. 5, to fine-tune the wavelength slightly. After the system is tuned and configured, it does not need further power, and the tuned states correspond to "memory" effects. In the setup, the MRR's free spectral range (FSR) is 6.8 nm. Furthermore,

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if the channel spacing is matched to the wavelength shift of the ON/OFF states, one FSR can contain up to 16 channels.

5. Summary

In this study, we proposed a non-volatile PMC for memory-functionality in silicon photonics integrated circuits. Our device was fabricated using CMOS-compatible processes, and electrical program and erase functions were experimentally demonstrated. As an example, we illustrated an add/drop MRR affording up to 65 states of multi-level memory functions. A 4-channel programmable non-volatile WDM circuit was used to highlight the functionality of our device. Our findings indicate that the memory waveguide structure can be applied to functional devices such as modulators, variable optical attenuators (VOAs), and even photonic crystals with memory functions. Meanwhile, multi-level memory components can be of interest in machine learing systems, with different levels corresponding to different memory depths. In conclusion, our technique can equip memory functions to optical chips, affording “intelligent” optical chips.