First demonstration of CMOS compatible electrical programmable photonic memory cell

Junfeng Song,[1,2] Andy Eu-Jin Lim,[1] Xianshu Luo,[1] Qing Fang,[1] Chao Li,[1] Lianxi Jia,[1] Xiaoguang Tu,[1] Ying Huang,[1] Tsung-Yang Liow,[1] and Guoqiang Lo[1]

*[1]Institute of Microelectronics, A*STAR (Agency for Science, Technology and Research) 11 Science Park Road, Singapore Science Park II, Singapore 117685.*

[2]State Key Laboratory on Integrated Opto-Electronics, College of Electronic Science and Engineering, Jilin University, Changchun, China, 130023

Email: songjf@ime.a-star.edu.sg

Abstract: We propose an electrically programmable, multi-level non-volatile photonics memory cell (PMC) fabricated by standard CMOS compatible processes. A micro-ring resonator (MRR) was built using the PMC to demonstrate programmable and erase functions.

OCIS codes: (210.4770) Optical recording; (210.4810) Optical storage-recording material; (250.3140) Integrated optoelectronic circuits; (130.3120) Integrated optics devices; (130.4815) Optical switching device

1. Introduction

Silicon photonics circuits are playing increasingly important roles in optical communication and interconnect fields [1,2]. However, conventional integrated optical waveguide is without memory functionality. Therefore, refractive index changes within an optical waveguide is required to maintain the state of the waveguide in devices such as optical switches and modulators [3,4]. This results in large energy consumption during operation. Here we design and demonstrate experimentally an electrically programmable and erasable, non-volatile optical waveguide memory structure. Using electrical voltage pulses, the waveguide state is changed while no energy is required to maintain the optical memory state. This novel optical memory waveguide structure can be utilized to have significant impact on various applications in optical interconnects, memory input/output interfaces, and neural networking.

2. Working principles

Figure 1 shows the proposed photonics memory cell (PMC) with programmable and erasable memory functions. The device utilizes a floating gate (FG) transistor structure with the source and drain separated. The left dished line box in Fig. 1 represents the optical waveguide with a polycrystalline-silicon (poly-Si) floating gate, separated by a thin oxide dielectric. At the source side (right dished line box), a poly-Si control gate overlaps the floating gate partially, and is separated from the floating gate by an oxide-nitride-oxide (ONO) stack.

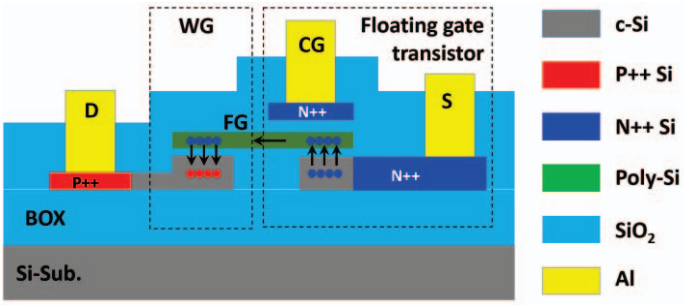

Fig. 1 Cross section illustration of the optical waveguide structure. WG: waveguide. FG: floating gate. CG: control gate. S: source. D: drain.

Program (*write*)

By applying voltage to electrical source (S) and control gate (CG), electrons acquire sufficient energy to tunnel through the gate oxide and into the floating gate. By controlling the FG doping profile and drain (D) voltage, while keeping source and CG un-biased, the electrons will be transported to the drain side of the FG. The injected carriers create a change the effective index of optical waveguide, and subsequently a phase change to the optical signal. This is labeled as the ON state in this work.

Erase

By setting the CG voltage to 0 V and biasing the drain terminal with a voltage, the electrons in the FG have enough energy to tunnel through the barrier between FG and bottom Si interface. The movement of electrons out from the FG will result in an optical phase change to the waveguide and this is classified to be the OFF state.

978-1-943580-11-8/16/$31.00 ©2016 Optical Society of America

3. Results and discussion

The devices were fabricated using standard CMOS technology in a 248 nm line. The Si waveguide is a 160 nm thick with a 100 nm slab. The tunneling gate oxide is 8 nm. The ONO stack consists of 6 nm TEOS oxide, 3.5 nm LPCVD Si_3N_4 and 6 nm TEOS oxide. Figure 2 shows the optical and SEM images of the MRR structures. We investigate the evolutionary program steps by supplying square-shaped electrical signals beginning from the OFF state. The signals have a peak voltage of 20 V with different pulse widths from 0 ms to 500 ms in steps of 25 ms. Figure 3a (top plot) shows the transmission spectra with increasing voltage pulse widths, and the bottom plot shows the corresponding resonance wavelengths. The efficiency of the resonance wavelength shift is ~ 2.53 pm/ms. Figure 3b shows the results of the erase steps starting from the ON state. The same pulse widths were used, while the peak voltage was reduced to 6 V. The efficiency of the red shift resonance associated to the erase step is 2.98 pm/ms. This occurs when the pulse width is larger than 50 ms and saturates at 200 ms. The step-like nature of the memory MRR can be useful in multi-level memory functionality. The endurance test of 30 cycles, and retention of 20 hrs was also conducted for both ON/OFF states.

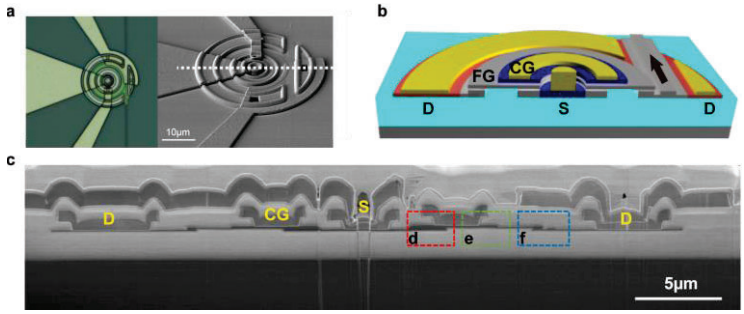

Fig. 2. Memory integrated silicon reconfigurable microring. **a,** optical and SEM picture of MRR PMC. **b,** Perspective view of the microring resonator integrated with memory optical waveguide, and coupled with a ridge optical bus waveguide. **c,** cross-sectional SEM of MRR PMC. **d,** The zoom-in TEM of control gate, floating gate and source. **e**, IPD (what is this) with control gate and floating gate, **f,** coupler of MOS optical waveguide and ridge waveguide.

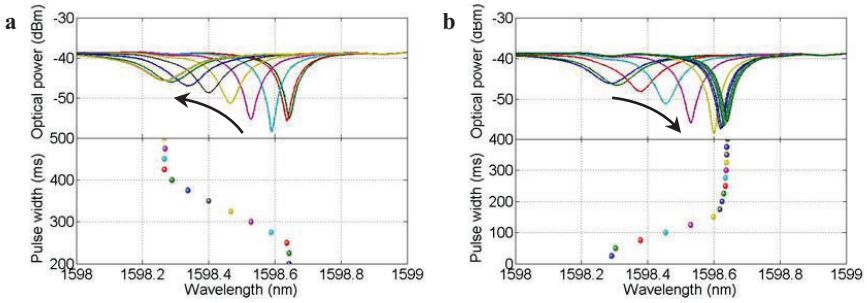

Fig. 3 Resonance wavelength evolutions upon square-shaped pulse voltage supply. **a,** Spectra evolution during program process upon square-shaped pulse voltage supply with increased pulse width starting from OFF state. **b,** Spectra evolution during erase process upon square-shaped pulse voltage supply with increased pulse width starting from ON state. The pulse width increases with step of 25 ms.

4. Summary

We proposed a novel silicon photonics memory cell using CMOS compatible processes. The device is shown to be electrically programmable and erasable by integrating it in a MRR. Endurance and retention tests were also conducted to demonstrate its stability and applicability in various photonics related applications.

Acknowledgement

This work was supported by program of National Natural Science Foundation of China (NSFC) under Grant Nos. 61177090 and 61377048.

5. References

[1] Y. Arakawa, T. Nakamura, Y. Urino, and T. Fujita, Silicon photonics for next generation system integration platform. *IEEE Commun. Mag.* **51,** 72-77 (2013).
[2] A. E.-J. Lim, *et al.* Review of silicon photonics foundry efforts. *IEEE J. Sel. Top. Quantum Electron.* **20**, 405-416 (2014).
[3] P. Dong, et.al., "Wavelength-tunable silicon microring modulator," Opt. Express **18**, 10941 (2010).
[4]X. Tu, T. -Y Liow, J. Song, X. Luo, Q. Fang, M. Yu, and G.-Q. Lo, "50-Gb/s silicon optical modulator with travelingwave electrodes," Optics express, **21**, 12776-12782 (2013)