3D Electro-Optical Integration Based on High-Performance Si Photonics TSV Interposer

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Abstract: 3D electro-optical integration based on a Cu-based Si-photonics TSV interposer has been demonstrated for integrated optical communication applications. The photonics TSV interposer consisting of monolithically integrated TSV, modulators and photodetectors, enabling a 30 Gbps-data-rate.

OCIS codes: (250.3140) Integrated optoelectronic circuits; (250.7360) Waveguide modulators; (230.5160) Photodetectors.

1. Introduction

A multi-functional optical communications platform requires both photonic integrated circuits (PIC) and CMOS electronics circuits to be integrated in the same system. For improved power efficiency and bandwidth densities of PIC, monolithic integration of CMOS circuits and Si photonic functional blocks has been explored and demonstrated recently [1]. However, this approach requires sophisticated co-integration electronic design automation (EDA) tool and processing skills to integrate them together on the same silicon chip. Consequently, it is difficult to achieve high overall yield [2]. Moreover, the huge mismatch in size between CMOS and photonics functional blocks is another disadvantage of the monolithic integration approach. The large footprint of Si photonics blocks easily takes up most of the die space, leaving little space for other electronics functional blocks to be placed. Some researchers [2] have proposed to separate the fabrication of Si photonics and CMOS electronics, and finally integrate them together using through-silicon-via (TSV), which is a 3D TSV integration scheme.

In this work, the technology options/integration strategies of electro-optical integration based on Si photonic TSV interposer and flip-chip bonding technology are proposed and investigated as a 3D integration scheme. By means of vertical TVS interconnection through the Si interposer, this 3D integration scheme provides a shorter communication route and lower power dissipation, therefore offering a promising solution for the continued scaling of tera-scale communication systems. In terms of performance of the key active devices, Si modulators and Ge photodetectors (PDs) integrated in a Si photonics platform has made some progress. Some works has been published at 25 Gbps [3] and 30 Gbps-data rate [4]. Our group also reported a 40 Gbps Si PIC [5]. In this work, a transmission data rate of 30 Gbps of the 3D TSV integration module is achieved. The needed toolbox of high-performance 3D electro-optical integration based on RF Si photonics TSV interposer has been established.

2. Design and fabrication process

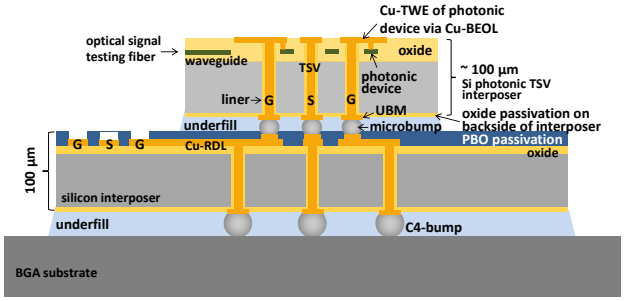

Fig. 1. Cross-sectional schematic of the 3D electro-optical TSV integration (not to scale).

The proposed 3D electro-optical TSV integration module is shown in Fig. 1. In this work, a Si photonic TSV interposer integrated is assembled on top of another bottom Si interposer. Active photonics devices, including monolithically integrated MZI modulatorand and Ge PD are designed and 100 µm-thick Si photonics TSV interposer. This photonics TSV is fabricated on a Si-on-insulator (SOI) substrate with 220 nm-thick top Si and 2 µm-thick buried oxide (BOX). The waveguide width is 500 nm and the slab height of the ridge waveguide is 100 nm

for modulator with 3 mm-long *PN* junction phase shifters. The doping compensations are utilized for optimizing the doping-induced optical loss and modulation speed [6]. The modulator fabrication process before metallization has been described in our reported modulator [6-7]. To reducing the Cu-induced optical loss and hence improving the responsivity of the Ge PD, discrete Cu contact plugs to Ge are employed as our reported design in [8]. The Ge waveguide PD thickness is 500 nm, and the length is 5 μm. The PD fabrication process before metallization has been established in our published paper [9].

TSV-middle process is implemented in the interposer before metallization of the photonic devices. After the contact plugs to Si and Ge were fabricated using Cu single-damascene process, TSVs shown in Fig. 2(a) were fabricated based on the process described previously in [10]. TSV keep-out-zone (KOZ) in Si photonics chip investigated in [10] has been accounted in the design phase. Depth of TSV 100 μm is designed based on capability of current thin wafer handling technology. For evaluating the microwave performance of the GSG-TSV, TSV diameter and pitch are optimized. Generally, smaller insertion/return loss can be achieved with the smaller TSV diameter and pitch. Finally 20 μm-diameter and center-to-center pitch of 100 μm TSVs with 1 μm-thick oxide liner are designed based on both optimization and fabrication conditions, which can provide a bandwidth of more than 40 GHz. Cu dual-damascene process was then employed to fabricate the traveling-wave electrode (TWE) and contact shown in Fig. 2(c)(d). The design, performance and process of the 2 μm-thick Cu TWE with a latticed surface pattern has been discussed in our reports [7-8]. TSVs' backside was revealed by back-grinding process, before backside oxide passivation layer was deposited for electrical isolation. Cu/Ni/Au under-bump-metals (UBMs) shown in inset i of Fig. 2(a) were fabricated using the ECP process. 3 μm-thick oxide dielectric layer, Cu-redistribution-layer (RDL) and Cu/Ni/SnAg microbumps were designed and fabricated on the bottom Si interposer, as shown in Fig. 2(a). Finally a flip-chip bonding technology for this 3D integration was developed based on the thermal compression bonding (TCB) method and vacuum reflow. The computed tomography (CT) image of the 3D TSV integration is given in Fig. 2(b), showing the TSV, Cu-TWE of the photonic device, microbump interconnects and Cu-RDL.

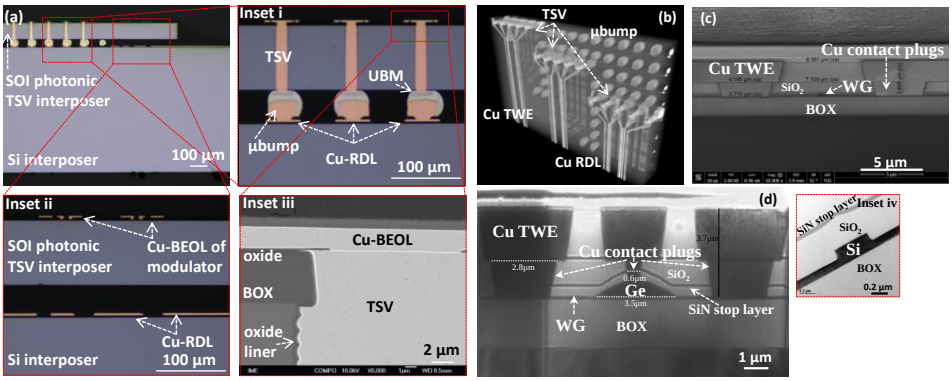

Fig. 2. (a) Cross-sectional images of the 3D EO integration module. Inset i: GSG-TSV and solder. Inset ii: Cu-TWE in photonics TSV interposer and Cu-RDL in Si interposer. Inset iii: Cu metallization of the Si photonics TSV interposer. (b) X-ray Computed Tomography (CT) image of the integration module. (c) Cross-sectional images of modulator. (d) Cross-sectional images of PD. Inset iv: Si waveguide.

3. Characterization results

Two lensed fibers with 2.5 μm focal-length were coupled to the nano-tip waveguide coupler in the photonic TSV interposer to characterize the optical performance of this 3D integration module. When the Cu-to-waveguide distance is more than 1 μm, the Cu-induced optical loss is < 0.25 dB/cm which can be negligible [7-8]. The measured output spectra of the modulator under different reversed biases on one arm are shown in Fig. 3, and the insertion loss is ~ 8 dB. With the reversed bias, the carrier is pumped out of the waveguide and the optical loss reduces. Thus, the optical extinction ratio decreases due to the unbalance of optical power in two modulator's arms with the increase of the reversed bias. Based on the undoped waveguide loss, the implantation-induced optical loss of 1.3 dB/mm is evaluated. A π-phase shift can be realized under 6.8 V reversed bias voltage for a 3 mm-long phase shifter, which corresponds to a modulation efficiency ($V_\pi \cdot L_\pi$) of 20.4 V·mm, as shown in Fig. 4. With an increase in the applied reversed voltage from −2 V to −10 V, the efficiency is reduced from 12.6 V·mm to 23.1 V·mm, which is caused by the depletion of free carriers in the *p-n* junction. Figure 5 is the responsivity results of Ge-on-Si PD with 5 μm-long Ge. Due to the special contact design of this PD, a responsivity of ~ 0.58A/W is achieved at 1550nm.

The RF signal was transmitted through the Cu-RDL, and then vertically transmitted through the microbumps/UBMs and the TSVs to drive the photonic devices. EO insertion loss S21 of the modulator and PD was

measured through Agilent Lightwave Component Analyzer (LCA). The modulator EO bandwidth is shown in Fig. 6. With the increase of the reverse bias, the EO 3-dB bandwidth of modulator increases. The 3-dB bandwidth of 20.1 GHz is achieved under V_{bias} = –5.0 V. The 3-dB bandwidth of this PD is shown in Fig. 7. At a reverse bias of –3V, a 28 GHz-bandwidth is realized. The integrated Cu-photonics interposer, consisting the above MZI modulator and Ge-on-Si PD, has 20 GHz transmission bandwidth when the integrated modulator and PD are operated with –5 V and –3 V reverse biases, respectively. Figure 8 shows the eye-diagram of 30 Gbps data rate of the integrated interposer. This data rate result is limited by our measurement setup. The total length of RF cable applied on the integrated circuit is ~ 1.5 m and the loss of a high-speed electrical signal is high in it. If the setup is much better, it is possible for this integrated circuit to get a data rate up to 40 Gbps.

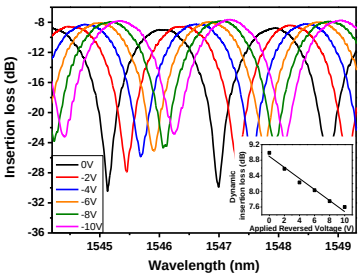

Fig. 3. Optical spectra of the MZI modulator.

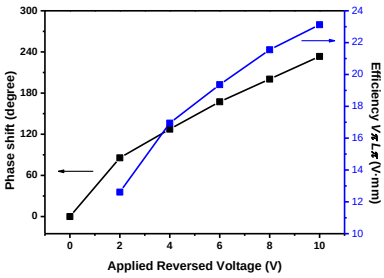

Fig. 4. Efficiency of the MZI modulator.

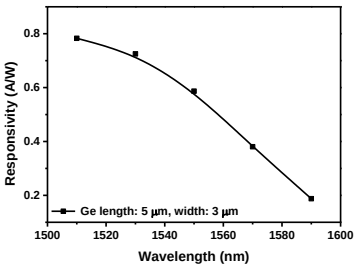

Fig. 5. Responsivity of the Ge PD.

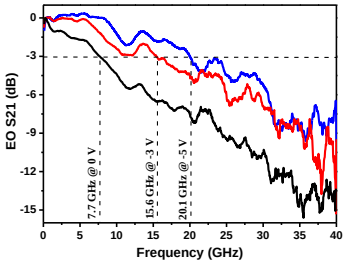

Fig. 6. Bandwidth of the MZI modulator.

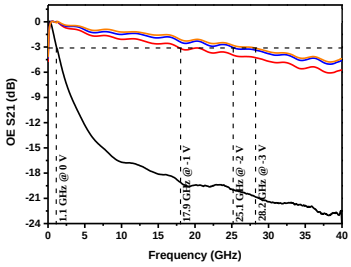

Fig. 7. Bandwidth of the Ge-on-Si PD.

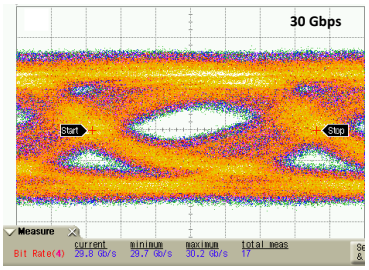

Fig. 8. 30 Gbps data rate of the 3D TSV integration module at λ=1550 nm.

4. Conclusion

We explore 3D electro-optical integration based on Si Cu-photonics TSV interposer consisting of monolithically integrated Si modulators, Ge PDs and TSV for integrated optical communication. 20 GHz-bandwidth and 28 GHz-bandwidth are enabled on the MZI modulator and Ge-on-Si PD integrated with TSV, respectively. A 30 Gpbs data rate is realized on the 3D TSV integration module. The fabrication process is developed, and the characterization results of the 3D electro-optical TSV integration are presented. This work has established the needed toolbox of high-performance 3D electro-optical integration based on RF Si photonics TSV interposer.

5. References

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