Low Loss (<0.2dB per transition) CMOS Compatible Multi-Layer Si_3N_4-on-SOI Platform with Thermal-Optics Device Integration for Silicon Photonics

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Abstract: A multi-layer Si_3N_4-on-SOI platform is demonstrated, achieving <0.2dB transition loss between layers over 70nm bandwidth. 0.8dB/cm propagation loss is measured for PECVD Si_3N_4 waveguide at λ=1580nm. Thermal-optic micro-ring filter is also integrated on the platform.
OCIS codes: (130.3120) Integrated Optics Devices; (230.7370) Waveguides; (250.5300) Photonic Integrated Circuits

1. Introduction

Silicon photonics technology has drawn extensive global research attention for optical communication, driven by its device compactness, low cost and monolithic integration with electronics devices. Recently, multi-layer platform has emerged to further advance the technology from the conventional silicon-on-insulator (SOI) platform [1-5]. The additional optical device layers could offer various revenues in terms of denser integration [1], lower loss [2], better fabrication tolerance [3] and device performance [4, 5]. The integration approaches can be broadly classified into two categories, using either back-end [1-2] or front-end process [3-5]. The back-end integration could simplify the fabrication, often at the expense of excess loss due to the prohibition of high temperature annealing. In this work, we present our recent development on the multi-layer Si_3N_4-on-SOI platform using CMOS-compatible back-end process. Silicon is used as the first (bottom) optical device layer, enabling seamless integration with our existing devices on the SOI platform [6]. Plasma enhanced chemical vapor deposition (PECVD) Si_3N_4 is deposited on top of the SOI wafer as the second (top) device layer, with a thin oxide spacer between them. Thermo-optic devices are also included, illustrating the platform's expandability to include active device integration. In addition, platform loss reduction through waveguide and transition coupler (TC) design will be discussed.

2. Integration Process Flow

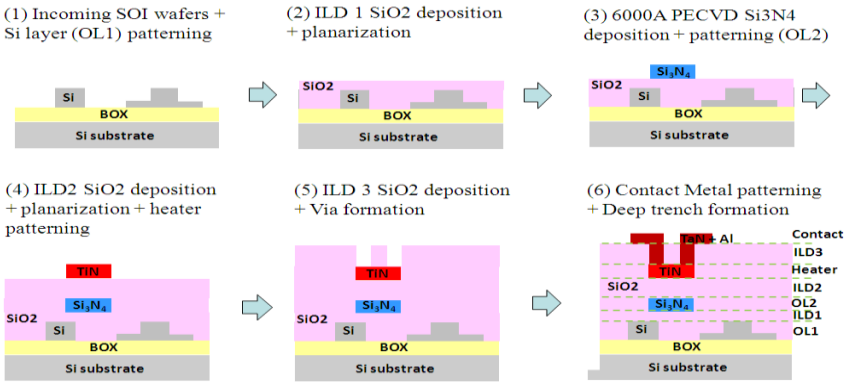

Fig. 1. Fabrication process flow for the Si_3N_4-on-SOI platform using back-end integration approach

Fig. 1 illustrates the integration process flow for the multi-layer Si_3N_4-on-SOI platform. The fabrication starts with an 8-inch SOI wafer with 220nm-thick top silicon layer and 3μm bottom oxide (BOX). Subsequent fabrication processes take place in a sequential manner: (1) first optical device layer (OL1) is formed in the top silicon layer, using DUV photolithography and reactive ion etching (RIE); (2) first SiO_2 layer (ILD1) is deposited, followed by planarization and thinning down to 100nm above the silicon layer; (3) second optical device layer (OL2) is formed on 600nm-thick PECVD Si3N4 deposited at low temperature (400°C); (4) second SiO_2 layer (ILD2) is deposited and planarized, followed by Titanium Nitride (TiN) heater deposition and patterning; (5) third SiO_2 layer (ILD3) is deposited for via formation; (6) Aluminum (Al) contact metal is formed, followed by bond pad (not shown in Fig. 1) and deep trench etching. Implantation and Germanium (Ge) epitaxial growth, which are needed to fabricate the high performance modulator and detector [6], can be incorporated between steps (1) and (3) in this process flow.

3. Experiments and Characterization

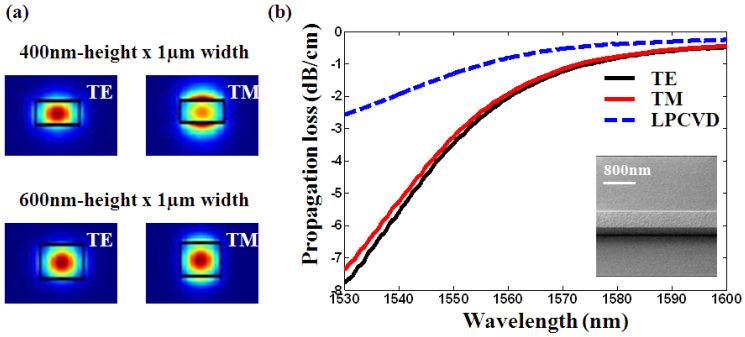

Fig. 2. (a) Simulated TE and TM modal profiles for 400nm-height and 600nm-height Si_3N_4 waveguides (b) propagation loss spectrum for the 600nm-height PECVD Si_3N_4 waveguide (inset: fabricated waveguide SEM images) for both TE (black) and TM (red) modes, the loss for 400nm-height LPCVD Si_3N_4 waveguide (dotted blue line) from earlier fabrication is also included for bench-marking purpose.

Waveguide loss remains as a major challenge for the back-end approach using PECVD Si_3N_4 deposited at 400°C, due to the poorer film quality compared to its high-temperature low pressure CVD (LPCVD) counterpart [7]. We look into addressing the challenge in this work by increasing the film thickness. Fig. 2 (a) illustrates the transverse-electric (TE) and transverse-magnetic (TM) mode profiles, for both 400nm- and 600nm-height Si_3N_4 waveguide with 1μm-width. The larger waveguide cross-section ensures a smaller modal overlap with the sidewall, reducing the scattering loss. In addition, the lower aspect ratio is beneficial for waveguide birefringence reduction. We then proceed to characterize the propagation loss for the 600nm-height Si_3N_4 waveguide using cut-back method, as shown in Fig. 2 (b). The TE mode propagation loss of a 400nm-height LPCVD Si_3N_4 waveguide (dotted curve) from our earlier run is also included in Fig. 2(b) for bench marking. The measured propagation losses for the 600nm-height PECVD Si_3N_4 waveguide are ~0.8dB/cm for both TE and TM modes at λ=1580nm, which are lower than the reported results for the 400nm-height devices [1]. The loss is still higher than its LPCVD counterpart. Further loss reduction could be achieved through deposition condition [7] or process optimization [8]. The coupling losses from a 300nm-width taper tip to the lensed fiber are 1.4 and 1.5 dB/facet for TE and TM mode respectively.

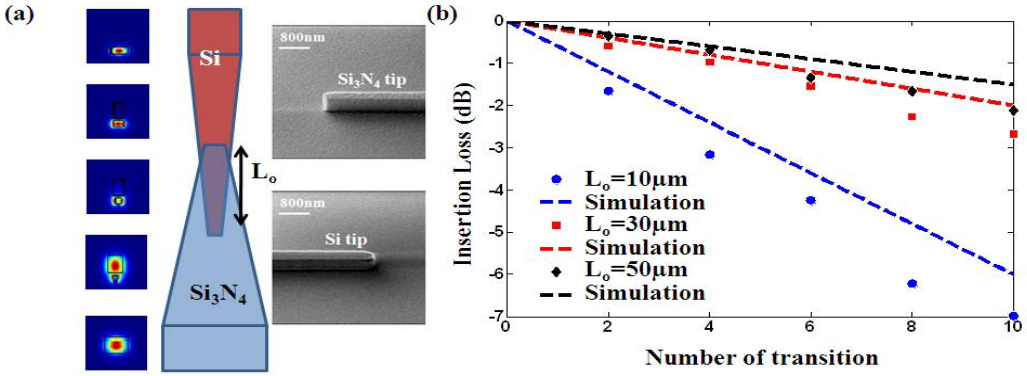

Fig. 3. (a) Center: schematic diagram of the TC between Si and Si_3N_4 device layer, left: TE mode profile evolution along the TC, right: SEM images of the fabricated tips in both layers; (b) measured (points) and simulated (dotted line) insertion loss for TC with different L_o length

Next, we investigate the transition loss between the two optical device layers. A transition coupler (TC) is designed for our particular platform, as shown in Fig. 3 (a). Waveguides in both layers are adiabatically tapered towards each other, with a tip width of 200nm and 300nm on the Si and Si_3N_4 layers, respectively. The SEM images of the fabricated tip in both layers are shown in Fig. 3(a). The mode evolution along the TC is also illustrated in Fig. 3 (a), which is simulated using finite element method (FEM). A short taper length of 50μm is chosen for both Si and Si_3N_4 layer, enabled by the thin oxide space (ILD 1) between them. Six sets of TC are fabricated, with an overlap length (L_o) of 0/10/20/30/40/50μm. The measured transition losses for three sets of the devices (points) are plotted in Fig. 3(b) for λ=1550nm, in good agreement with the simulation results using three dimensional (3-D) finite-difference-time-domain (FDTD) method (dotted line). The slight difference could be due to the lateral off-set introduced during the fabrication. In general, coupling loss decreases as we increase the overlap length (L_o). Optimal coupling loss of <0.2dB/transition occurs for L_o= 50μm, operating over a wide wavelength range from 1530nm to 1600nm. This is the lowest reported inter-layer transition loss in multi-layer platform up to today [2, 3].

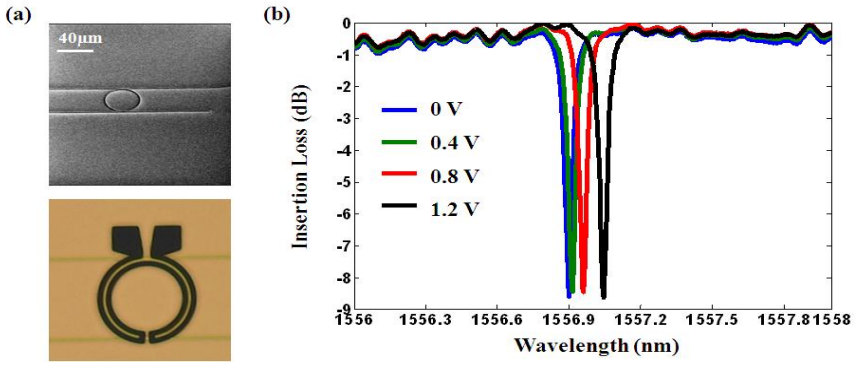

Fig. 4. (a) The SEM (top) and microscope (bottom) images of the micro-ring; (b) Transmission spectrum under different bias-voltage

To demonstrate the expandability of the platform to include active devices, a thermally tuned silicon micro-ring filter is fabricated. The SEM and microscope images of the fabricated devices are shown in Fig. 4(a). TiN heater is design to run in a dual-ring structure (black color in the microscope images). Fig. 4(b) shows the transmission spectrums for the 20μm-radius micro-ring filter, under different bias voltages. The quality factor (Q), calculated from the line-width, is > 30,000. The average insertion loss is less than 1dB. The thermal tuning efficiency is measured at ~0.11nm/mW. These results are comparable to a similar device fabricated on our SOI platform [9], justifying the platform's seamless integration capability for thermo-optic devices without performance degradation. Table 1benchmarks the performance of our Si_3N_4-on-SOI platform with the other reported multi-layer platforms.

Table 1. Performance benchmarking of reported multi-layer platforms for silicon photonics

Group	Optical Layer 1 (OL1)	Optical Layer 2 (OL2)	OL1 waveguide loss	Inter-layer loss (per transition)	Active integration
[1]	400nm PECVD Si_3N_4	400nm PECVD Si_3N_4	1dB/cm @1580nm	N.A.	No
[2]	100nm LPCVD Si_3N_4	500nm Si	1.2dB/m @1590nm	>0.4dB	No
[3]	400nm LPCVD Si_3N_4	220nm Si	N.A.	0.5dB	Ge PD
[4]	3μm SiO_x	200nm Si	0.57dB/cm @1550nm	<0.37dB	Si VOA
This work	600nm PECVD Si_3N_4	220nm Si	0.8dB/cm @1580nm	<0.2dB	Heater

4. Conclusion

In summary, we present the fabrication and characterization of a CMOS-compatible Si_3N_4–on-SOI platform using a back-end approach. 0.8 dB/cm propagation loss is achieved with a 600nm-height PECVD Si_3N_4 waveguide at λ=1580nm. Ultra-low transition loss of < 0.2dB/transition is measured over 70nm-bandwidth, using maximally overlap adiabatic tapers in both layers. A thermally tuned micro-ring filter is also demonstrated on the platform, with Q > 30,000 and 0.11nm/mW thermal tuning efficiency. These preliminary results validate the feasibility and capability of the presented platform to further advance silicon photonics technology from the current SOI platform.

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