Path to Silicon Photonics Commercialization: 25 Gb/s Platform Development in a CMOS Manufacturing Foundry Line

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Abstract: Silicon photonics platform in a commercial 0.18 µm CMOS foundry line is described. Low-loss Si passives and high speed germanium photodetectors (>20GHz) with low dark current (~11nA) and high responsivity (1.06A/W) at 1550nm are presented.

OCIS codes: (230.0230) Optical devices; (250.0250) Optoelectronics

1. Introduction

Silicon photonics has become one of the leading technological solutions for integrated photonics that target applications such as high performance computing, optical communications (telecom/datacom), optical sensors, and on-chip optical interconnects. Over the last two decades, silicon photonics technology has reached new heights in terms of device performance and levels of integration. This has garnered vast interest in the field due to its tremendous market potential. Recent acquisitions of silicon photonics companies indicate an inflexion point for commercialization in the coming years [1] – [3]. At this critical juncture, unless concerted efforts are made to develop foundry lines for prototyping and chip fabrication in a high yield manufacturing environment, the vision of 'low-cost' silicon photonics may take considerably longer to realize. In this paper, we describe a silicon photonics integrated platform development in a 0.18 µm CMOS manufacturing line at GlobalFoundries (GF), Singapore. Interim results for two important modules (the Si passives and waveguided Ge *pin* PD) in this transfer are presented.

2. Integrated Silicon Photonics Platform

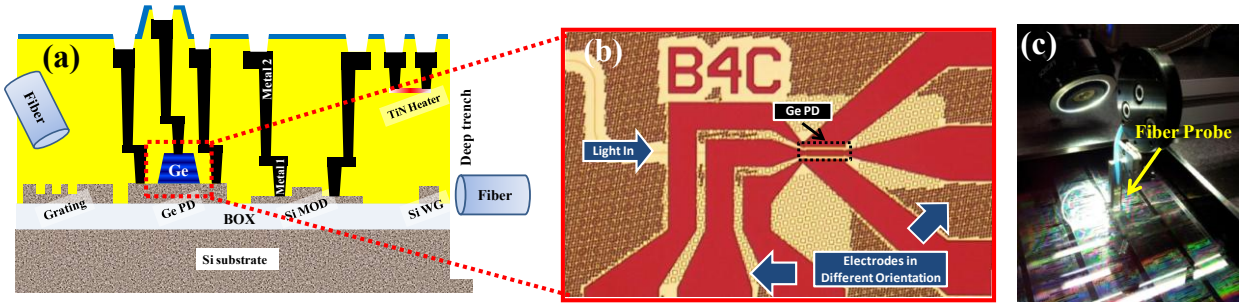

Fig.1: (a) Schematic of silicon photonics platform set-up in GF's 0.18 µm CMOS foundry line (b) Optical image of a Ge PD (after metal 1) fabricated in GF. (c) Wafer-level optical tester used for photonics device characterization.

The technology development was done on GF's 200 mm 0.18 µm CMOS foundry line used for high volume manufacturing. This manufacturing line is leveraged to provide low-cost, high-yield processing capabilities for the fully-integrated silicon photonics platform. A post-etch final inspection critical dimension (FICD) of 250.3 +/- 4.86 nm (Mean +/- Stdev) with Cp(Cpk) of 2.06(2.03) is typical of a 0.18 µm CMOS wafer (for a 250 nm CD target). This gives an indication of the strict process controls achievable from the manufacturing facility.

A 220 nm Si/ 3 µm buried oxide (BOX) high resistivity silicon-oxide-insulator (SOI) wafer was used as the starting substrate. The Si passives fabrication process involved two partial etches; one for a 70 nm grating etch depth and another for a 90 nm slab thickness in a Si rib waveguide (WG). After the two partial etches, a third Si etch to the BOX was used to complete the passives formation. Multiple Si implants were conducted before Ge epitaxy, while a n++ Ge implant was done afterwhich. GF's standard back-end-of-line (BEOL) process consisting of tungsten (W) plugs and Aluminum (Al) metal was used for a two-level metallization. A TiN heater was integrated between the two metal levels for thermal-optic tuning/modulation. Inter-layer dielectric (ILD) and inter-metal dielectric (IMD) was purely oxide. This minimizes dispersion due to dielectric material refractive index differences and interface effects during surface coupling. A silicon nitride top layer was used for passivation and can be optionally removed at areas where efficient surface coupling is required.

A full suite of photonic devices covering, but not limited to, low-loss Si passives, vertical *pin* germanium photodetectors (Ge PD), Mach-Zehnder (MZ) *pn* Si modulators (MOD), TiN heater for thermal-optics, and efficient

couplers are supported on this technology platform [see Fig. 1 (a)]. One core capability of the platform is the suspended oxide coupler which allows large fiber-to-chip alignment tolerance and is particularly useful for high-speed photonic packaging needs [4]. Process modules were individually verified for functionality during the technology transfer to ensure photonic devices meet specifications before full integration. Fig. 1 (b) shows a Ge PD fabricated in GF's CMOS line after Metal 1. For electronic-photonic integration, GF's basic wire-bonding or bump-bonding (flip-chip) bond pad design rules could be utilized.

3. Results & Discussion

(a) Low-loss Si Passives

A Si passive wafer (with a full oxide cladding thickness of 6 µm) was fab out from GF's line and measured using a wafer-scale optical tester [Fig. 1(c)]. Figure 2 shows the wafer-scale measurements conducted for Si channel and rib WGs of width 500 nm. Channel and rib WG propagation loss of ~1.66 dB/cm and ~1.09 dB/cm were attained at central wavelength, respectively. Tight optical loss distributions with standard deviation of ~0.2 dB/cm were obtained for both WGs from the first pilot wafer. Bending loss for a 5 µm Si channel WG bend (width of 500 nm) was also measured to be 0.014 dB per 90° bend. The mean (and median) central wavelength for this wafer was at 1541 nm. In these measurements, the SiN layer was not removed above the gratings. These gratings were not optimized for best efficiency (with coupling loss of ~6 dB), since they were primarily used for wafer-level testing. The coupling efficiency could be improved by 50% using non-uniformed grating couplers on the same top Si thickness of 220 nm [5]. Measurements at 1550 nm were also extracted for these passives and gave similar losses and distributions.

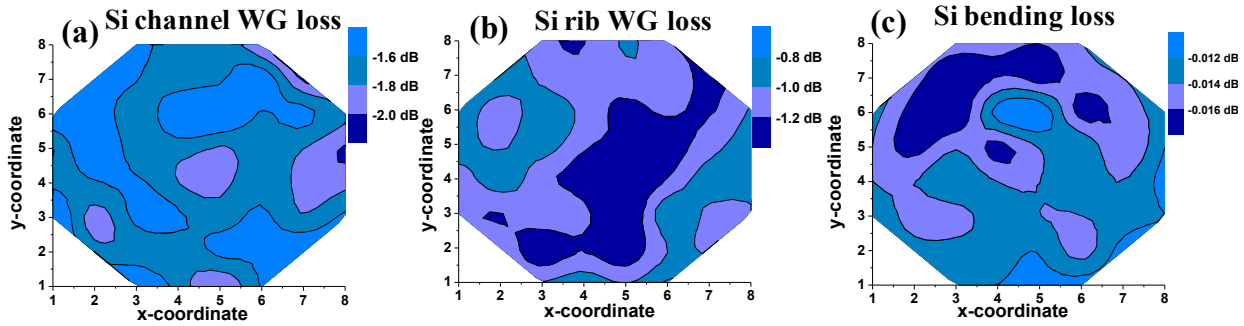

Fig.2: Wafer-level optical measurement for (a) Si channel WG (b) Si rib WG, and (c) Si 90 ° bends (5 µm radius) for a full wafer consisting 52 dies. Si passives were also verified at die-level (through edge coupling) from a lensed fiber and a 180 nm nanotaper with a coupling loss of 2 – 3 dB/facet.

(b) High Performance Ge Detectors

Waveguided vertical *pin* Ge PDs was fabricated on this platform using a specially-tuned epitaxy recipe. A Ge PD wafer was pulled out after Metal 1 for measurements to verify device performance. Statistical plots of dark current, forward current and capacitance for a 8 × 25 µm PD are shown in Fig. 3. The *IV* and *CV* uniformity were extremely good for the pilot wafer. Average dark current was ~11 nA at -1V reverse bias which gave a dark current density of ~5.5 mA/cm^2. The dark current density is one of the lowest reported for an integrated Ge PD [6] - [7] and indicates the low defectivity of the Ge epitaxial film. High forward current (~14.5 mA) to dark current ratio at ±1 V of ~10^6 was attained. The normalized capacitance per unit length was 1.1 fF/µm at -1V with a standard deviation of less than 2%. This confirmed that the Ge thickness uniformity in the epitaxy process and other PD related processes such as implant, dopant anneal, and contact etch were well-controlled. A total of 8 PDs with different dimensions and design variations were measured (for *IV* and *CV*) with 100% yield and similar distributions.

Light at 1550 nm wavelength from a tunable laser source (TLS) was coupled into the photodetector through the grating coupler. Due to the lack of a feedback loop from the photodetector (via an output grating coupler), fiber array alignment was done on a standard grating aligner structure before moving to the PD. No additional optical alignment was conducted after the fiber array moved to the input grating coupler of the detector. The grating ensured that only TE polarized light was input into the PD. Fig. 4 (a) shows the *IV* characteristics of the PD under dark and illuminated conditions. The photocurrent was more than 4 orders higher than the dark current at -1V. For internal responsivity calculations, the grating coupling loss and Si WG propagation loss were decoupled from the laser power to get the input power into the Ge PD. Average responsivity of 1.06+/-0.15 A/W at -1V reverse bias

was calculated (for a smaller sample size of 16 dies). 3 dB bandwidth measured was larger than 20 GHz at -1V at 1550 nm wavelength [Fig. 4(b)] and is sufficient for 25 Gb/s operation. The current detector design was that of a baseline control PD, and not optimized for higher bandwidth. The PD bandwidth could be further improved by direct scaling of the detector area to reduce the device capacitance. Detector responsivity is not expected to degrade through scaling given the "thick" Ge (> 500 nm) used for the PD.

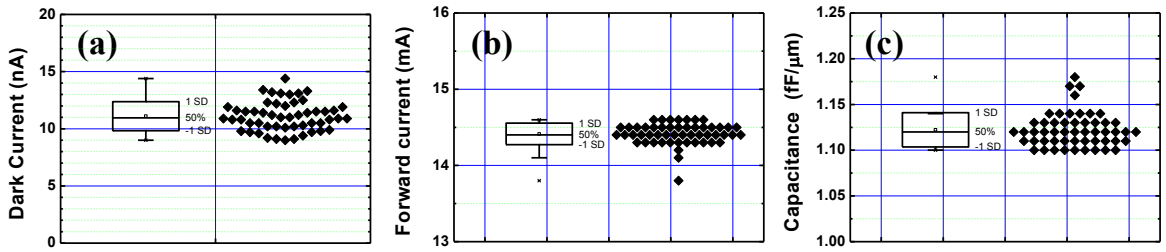

Fig.3: Statistical plots for dark current, forward current and normalized capacitance (at |1V|) for a 8 × 25 μm Ge PD showing excellent uniformity. This is the first time electrical yield statistics for a Ge PD manufactured in a commercial foundry is presented.

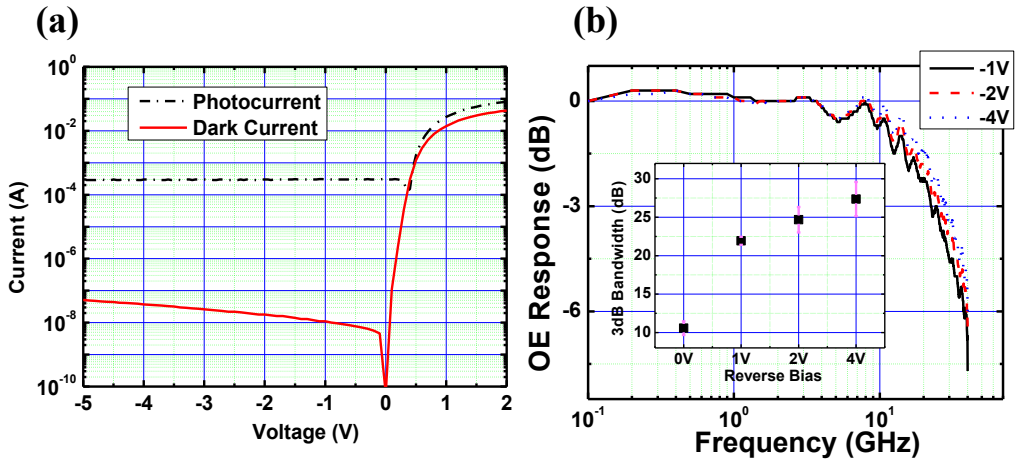

Fig 4. (a) *IV* characteristics of the 8 × 25 μm Ge PD under dark current (I_{dark}) and photocurrent (I_{photo}) conditions. I_{photo}/I_{dark} ratio larger than 4 orders of magnitude is obtained. (b) OE response at different reverse biases showing 3dB bandwidths that are >20 GHz. Inset plots the 3dB bandwidth for different reverse biases from 9 dies average.

4. Summary

A silicon photonics platform was developed in GlobalFoundries 0.18 μm CMOS manufacturing line. Important process modules such as low-loss Si passive and high performance Ge detectors were verified for functionality. Other photonics devices like the Si MOD, and TiN heater had already been integrated with the Si passives and Ge PD in a full flow, and would be presented in due course. This work serves as an enablement of silicon photonics prototyping and mass production needs in an accessible commercial foundry.

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