CMOS compatible monolithic multi-layer Si_3N_4-on-SOI platform for low-loss high performance silicon photonics dense integration

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Abstract: We demonstrated a low-loss CMOS-compatible multi-layer platform using monolithic back-end-of-line (BEOL) integration. 0.8dB/cm propagation loss is measured for the PECVD Si_3N_4 waveguide at 1580nm wavelength. The loss is further reduced to 0.24dB/cm at 1270nm wavelength, justifying the platform's feasibility for O-band operation. An inter-layer transition coupler is designed, achieving less than 0.2dB/transition loss across 70nm bandwidth. This is the lowest inter-layer transition loss ever reported. A thermally tuned micro-ring filter is also integrated on the platform, with performance comparable to similar device on SOI platform.

OCIS codes: (230.3120) Integrated optics devices; (130.0130) Integrated optics; (230.7370) Waveguides.

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1. Introduction

Silicon photonics technology has drawn extensive global research attention for optical communication, driven by its device compactness, low cost and potential monolithic integration with electronics devices. The technology advancement has been largely relied on the silicon-on-insulator (SOI) platform over the past decade, with the demonstration of high performance passive devices, modulators, photo-detectors and their integration for complex photonic functionality [1, 2]. As optical interconnect technology moves towards application demanding ultra-fast speed and dense integration, conventional SOI platform rapidly becomes insufficient due to its limitation in on-chip space, loss, fabrication tolerance and flexibility [3]. Multi-layer platforms could provide the answer to address these performance bottlenecks, taking advantages of the three-dimentional integration nature and material versatility. The additional optical device layers offer various revenues in terms of denser integration [4], lower loss [5], better device performance [6–8] and fabrication tolerance [9]. The inclusion of relative low index contrast waveguide, using silica or Si_3N_4, could also benefit Quantum photonics application requiring precise device performance control [10].

The integration approaches for multi-layer platform can be broadly classified into two categories, using either back-end-of-line (BOEL) [4–6] or front-end-of-line (FEOL) process [7–9]. The main difference comes from the deposition temperature of the optical device layer material, resulting in the trade-off between platform loss and fabrication complexity. The BEOL approach provides excellent vertical scalability with its simple integration flow, often at the expense of excess loss due to the prohibition of high temperature annealing. Various innovative techniques have been proposed to address it, using wafer bonding [5] or different optical layer material [6]. The solutions are however far from satisfactory, due to the increased process complexity and device foot print. These approaches also post significant difficulty when comes to active device integration and scale-up for more optical layers. In this work, we present our recent development on the multi-layer Si_3N_4-on-SOI platform using CMOS-compatible back-end process. In particular, platform loss reduction will be investigated systematically, in terms of both the propagation loss and inter-optical layer transition loss. Single-crystal silicon from SOI wafer is chosen as the first (bottom) optical device layer, enabling seamless integration with our existing device library [11]. Superior performance could be obtained with respect to its deposited-Si counterpart, for both passive [12] and active devices [13]. Plasma enhanced chemical vapor deposition (PECVD) Si_3N_4 is deposited on top of the SOI wafer as the second (top) device layer, with a thin oxide spacer between them. Thermo-optic devices are also included, illustrating the platform's expandability to include active device integration.

2. Integration process flow for Si_3N_4-on-SOI multi-layer platform

Figure 1 illustrates the integration process flow for the multi-layer Si_3N_4-on-SOI platform. The fabrication starts with an 8-inch SOI wafer with 220nm-thick single crystal silicon layer and 3μm bottom oxide (BOX). Subsequent fabrication processes take place in a sequential

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manner: (1) first optical device layer (OL1) is formed in the top silicon layer, using two steps of DUV photolithography and reactive ion etching (RIE); (2) first PECVD SiO_2 layer (IDL1) is deposited, followed by chemical-mechanical polishing (CMP) planarization and thinning down to 100nm above the silicon layer; (3) second optical device layer (OL2) is formed on 600nm-thick PECVD Si_3N_4 deposited at low temperature (400°C), followed by DUV photolithography and one-step RIE full etch stop on oxide; (4) second SiO_2 layer (IDL2) is deposited and planarized, followed by Titanium Nitride (TiN) heater formation; (5) third SiO_2 layer (IDL3) is deposited for via formation; (6) Aluminum (Al) contact metal is formed, followed by bond pad (not shown in Fig. 1) and deep trench etching. ILD 2 thickness was 1μm, to ensure minimal excess loss and maximal heater efficiency. The sequential deposition-based integration flow will facilitate straight-forward vertical scale-up to incorporate more optical layers. We noted here that the 100nm-thin oxide spacer might post some layout constraint due to the potential cross-talk. This however should not compromise the integration density significantly, given the weak cross-coupling and potential for further photonic layers stacking. Implantation, Germanium (Ge) epitaxial growth for high performance active devices [11], and lateral under-cut trench for thermal isolation [14] and suspended spot size converter [15] are not included in the current work. They can be incorporated before IDL1 deposition and deep trench fabrication, respectively in the integration flow.

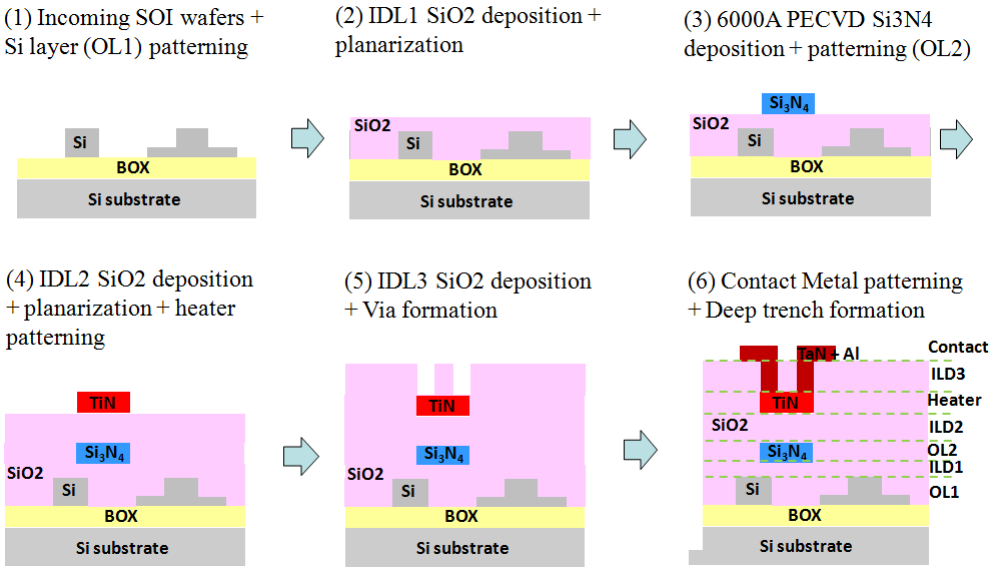

Fig. 1. Fabrication process flow for the Si_3N_4-on-SOI multi-layer platform using back-end integration approach.

3. Experiments and result discussion

Waveguide loss remains as a major challenge for the back-end approach using PECVD Si_3N_4, due to the low thermal budget requirement. The prohibition of high temperature to drive out the N-H bonds results in high absorption loss near 1.5μm wavelength, as compared to its high-temperature low pressure CVD (LPCVD) counterpart [16]. The high propagation loss severely limits the available link-budget of the platform, reducing its scalability. In this work, we look into two approaches to address this challenge, in an attempt to reduce both the scattering and absorption loss. To suppress the scattering loss, we proposed to increase the film thickness. Figure 2(a) illustrates the transverse-electric (TE) and transverse-magnetic (TM) mode profiles, for both 400nm- and 600nm-height Si_3N_4 waveguide with 1μm-width. The larger waveguide cross-section ensures a smaller modal overlap with the sidewall, reducing the scattering loss. In addition, the lower aspect ratio is beneficial for waveguide

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birefringence reduction. Further film thickness will yield insignificant loss suppression, while inducing higher order mode and via opening process complexity. We then proceed to characterize the propagation loss for the 600nm-height Si_3N_4 waveguide using cut-back method, as shown in Fig. 2(b). Co-plotting curves on the graph are the Si waveguide TE mode propagation loss on the multi-layer platform, as well as 400nm-height LPCVD and PECVD Si_3N_4 waveguide TE-mode propagation losses from our earlier runs. The loss values are summarized in Table 1, for both 1550nm and 1580nm wavelengths. The coupling losses from a 300nm-width Si_3N_4 taper tip to the lensed fiber are 1.4 and 1.5 dB/facet for TE and TM mode respectively. The measured propagation losses for the 600nm-height PECVD Si_3N_4 waveguide are ~0.8dB/cm for both TE and TM modes at λ = 1580nm. This is ~0.3dB lower than the results for the 400nm-height devices, justifying its capability to suppress scattering loss. Such low propagation loss will enable our platform to operate in the 1580nm and beyond wavelength range. On the other hand, the loss suppression effect becomes insignificant in the 1550nm wavelength, due to the dominance of scattering loss.

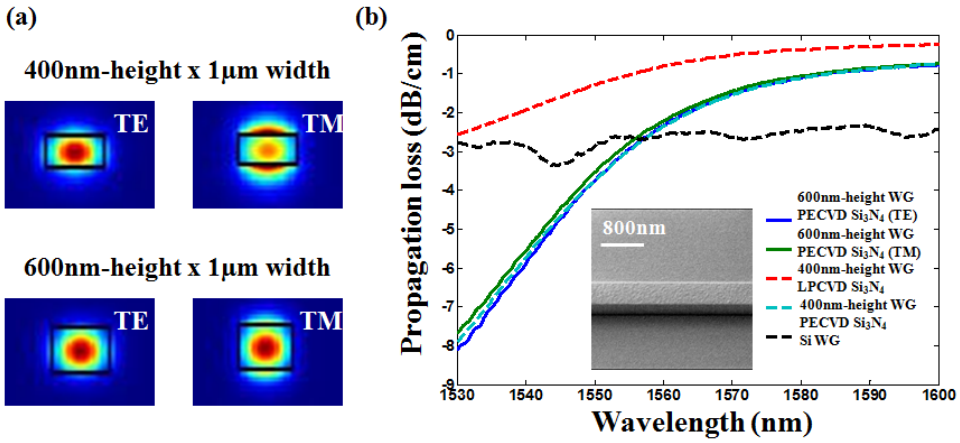

Fig. 2. (a) Simulated TE and TM modal profiles for 400nm-height and 600nm-height Si_3N_4 waveguides; (b) propagation loss spectrum for the 600nm-height PECVD Si_3N_4 waveguide (inset: fabricated waveguide SEM images) for both TE (blue) and TM (green) modes, the loss for Si waveguide (black) on the platform. The loss for 400nm-height PECVD (light blue) and LPCVD (red) Si_3N_4 waveguide from earlier fabrication is also included for comparison.

Table 1. Propagation Loss Comparison for Si, LPCVD and PECVD Si_3N_4 Waveguides

Wavelength	Si	400nm-height LPCVD Si_3N_4	400nm-height PECVD Si_3N_4	600nm-height PECVD Si_3N_4
1550nm	2.85 dB/cm	1.3 dB/cm	3.75 dB/cm	3.5 dB/cm
1580nm	2.5 dB/cm	0.4 dB/cm	1.1 dB/cm	0.8 dB/cm
1270nm	5.5dB/cm	0.32dB/cm	0.45dB/cm	0.24dB/cm

Despite the scattering loss suppression, propagation loss for PECVD Si_3N_4 waveguide remains much higher than its LPCVD counterpart. This is mainly due to the large absorption loss, originated from the presence of N-H bond in PECVD Si_3N_4 film. Optimized film deposition with low hydrogen module could partially solve this problem [16]. A more direct approach is to move away from the N-H bond absorption peak, by routing optical signals in the 1310nm wavelength windows. O-band operation is also preferred for applications like Ethernet and data center interconnect, which has gained increasing interest within the silicon photonics community over the recent years [17]. Figure 3 plots the TE mode propagation losses from various waveguide materials in the 1310nm wavelength window, and their values at λ = 1270nm are summarized in the last row of Table 1. We note here that the high Si waveguide loss could be due to the 500nm waveguide width, as devices operating in the 1310nm wavelength typically use narrower waveguide [18]. The propagation loss for 600nm-height Si_3N_4 waveguide remains less than 0.45dB/cm over the entire spectrum, comparable

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with its LPCVD counter-part. The loss is 0.24dB/cm @ 1270nm wavelength, more than an order of magnitude lower than that in the 1550nm wavelength. The result justifies the significance of this approach to reduce absorption loss, and the potential of our multi-layer platform for Ethernet and data-com applications. We note here that this is the first characterization of multi-layer platform in the O-band, to the best of our knowledge. Further loss reduction could be achieved through process optimization [19].

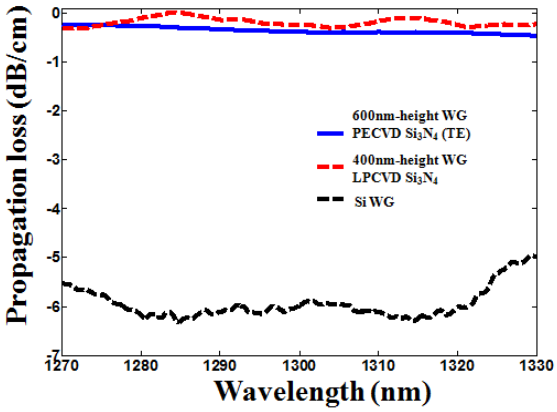

Fig. 3. TE mode propagation loss spectrum for the 600nm-height PECVD Si_3N_4 (blue), 400nm-height LPCVD Si_3N_4 (red) and Si waveguide (black).

Next, we look into the inter-layer transition loss (ILTL), which is the loss incurred when signals travel vertically across different optical layers. A low ILTS is essential for the scalability of the multi-layer platform, enabling architecture design freedom for complex system applications. . The schematic diagram of our transition coupler (TC) is shown in Fig. 4(a). Waveguides in both layers are adiabatically tapered towards each other, with a tip width of 200nm and 300nm on the Si and Si_3N_4 layers, respectively. Such structure is chosen due to its fabrication simplicity and low sensitivity to process variation. The SEM images of the fabricated tip in both layers are shown in Fig. 4(a). The mode evolution along the TC is also illustrated, which is simulated using finite element method (FEM). Three dimensional finite-difference-time-domain (3D-FDTD) is then carried out to optimize the device, particularly on the taper length and overlap length between two tapers (L_o). A short taper length of 50μm is found to be sufficient for both Si and Si_3N_4 layer, enabled by the thin oxide space (ILD 1) between them. The influence of L_o on the ILTS is plotted in Fig. 4(b). Minimum coupling loss occurs with the maximally overlapped tapers. In addition, the loss is less than 0.25dB/transition for L_o>20μm. This is desirable to ensure large fabrication tolerance for lateral offset between Si and Si_3N_4 layers. 3D-FDTD simulation also confirms that typical horizontal offset introduced in our scanner (± 60nm) incurs negligible excess loss to the TC. Six sets of TC were subsequently fabricated, with an overlap length (L_o) of 0/10/20/30/40/50μm. Five devices are fabricated for each set, with 2/4/6/8/10 TC incorporated respectively. Their insertion losses are computed by normalizing to a straight waveguide, which are subsequently used to compute the ILTL using cut-back method. The measured transition losses for three sets of the devices (points) are plotted in Fig. 4(c) for λ = 1550nm, in good agreement with the simulation results (dotted line). The slight difference could be due to the vertical off-set introduced during the fabrication. Another possible reason could be the change of oxide spacer thickness, which was measured at 115 ± 15nm using in-line ellipsometer. Given the short development history of this platform, we believe better spacer thickness control could be achieved for future fabrications. Optimal coupling loss of <0.2dB/transition occurs for L_o = 50μm. We note here that this is the lowest reported inter-layer transition loss in multi-layer platform up to today [5, 6]. Figure 4(d) illustrates the transmission spectrum of the best and worst device. Both devices operate over a wide

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wavelength range from 1530nm to 1600nm, which is limited by our measurement set-up. We have also characterized our TC in the 1310nm wavelength window, as shown in the inset of Fig. 4(d). The ILTL is < 0.2dB/transition over the entire measurement windows from 1270nm to 1330nm, which is limited by our measurement set-up.

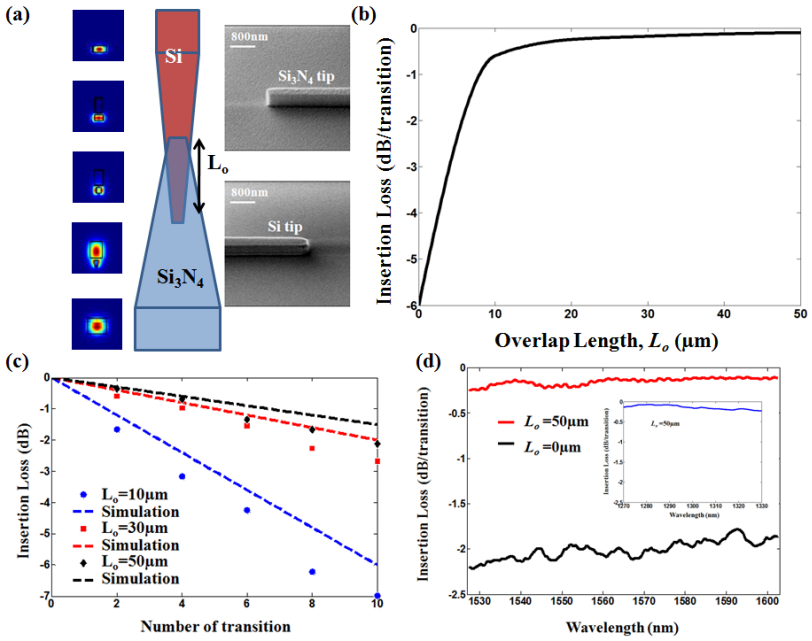

Fig. 4. (a) Center: schematic diagram of the TC between Si and Si_3N_4 device layer, left: TE mode profile evolution along the TC, right: SEM images of the fabricated tips in both layers; (b) Stimulated (3D-FDTD) transition loss with respect to overlap length L_o; (c) Measured (dots) and simulated (dotted line) insertion loss of TC with different overlap length; (d) ILTL spectrum for the best (red) and worse (black) TC, inset: best TC at 1310nm wavelength.

As a first step to demonstrate the expandability of the platform to include active devices, a thermally tuned silicon micro-ring filter is fabricated. Another incentive to choose this device is due to its high sensitivity to fabrication variation, to exanimate the influence of the multi-layer platform process over-head on the SOI layer devices. The SEM and microscope images of the fabricated devices are shown in Fig. 5(a). The micro-ring sits on the SOI layer, with a radius of 20μm. TiN heater is design to run in a dual-ring structure (black color in the microscope images), to be consistent with our earlier work for comparison purpose [20]. Figure 5(b) shows the transmission spectrums for the micro-ring filter, under different bias voltages. The quality factor (Q), calculated from the line-width, is > 30,000. The average insertion loss is less than 1dB. By linearly fitting the resonance wavelength shift with respect to the input electrical power, the thermal tuning efficiency is measured at ~0.11nm/mW. These results are all comparable to a similar device fabricated on our SOI platform [20], justifying the platform's seamless integration capability for thermo-optic devices without performance degradation. Table 2 benchmarks the performance of our Si_3N_4-on-SOI platform with the other state-of-the-art multi-layer platforms.

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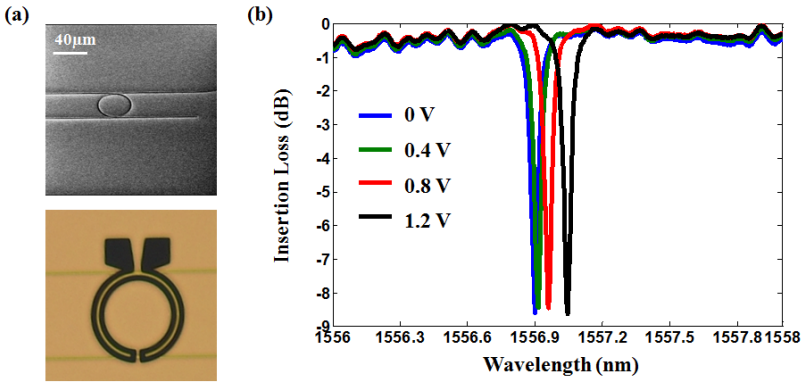

Fig. 5. (a) The SEM (top) and microscope (bottom) images of the micro-ring; (b) Transmission spectrum under different bias-voltage.

Table 2. Performance Benchmarking with State-of-the-art Multi-layer Platforms

Group	Optical Layer 1 (OL2)	Optical Layer 2 (OL1)	OL2 waveguide loss	Inter-layer loss (per transition)	Active integration
[4]	400nm PECVD Si_3N_4	400nm PECVD Si_3N_4	1dB/cm @1580nm	N.A.	No
[5]	100nm LPCVD Si_3N_4	500nm Si	1.2dB/m @1590nm	>0.4dB	No
[6]	3μm SiO_x	200nm Si	0.57dB/cm @1550nm	<0.37dB	Si VOA
[7]	400nm LPCVD Si_3N_4	220nm Si	N.A.	0.5dB	Ge PD
This work	600nm PECVD Si_3N_4	220nm Si	0.8dB/cm @1580nm 0.24dB/cm @1270nm	<0.2dB	Heater

5. Conclusions

In summary, we presented the fabrication and characterization of a CMOS-compatible Si_3N_4–on-SOI platform using a back-end approach. By suppressing the scattering loss, 0.8 dB/cm propagation loss is achieved with a 600nm-height PECVD Si_3N_4 waveguide at λ = 1580nm. An inter-layer transition coupler is designed on the platform. Ultra-low transition loss of < 0.2dB/transition is measured over 70nm-bandwidth, which is the lowest loss among all reported inter-layer transition coupler. We have also characterized the platform for O-band operation, with 0.24dB/cm propagation loss and 0.2dB/transition ILTL. Furthermore, a thermally tuned micro-ring filter is demonstrated on the platform, with Q > 30,000, insertion loss < 1dB, and thermal tuning efficiency of 0.11nm/mW. These preliminary results validate the feasibility and capability of the presented platform to further advance silicon photonics technology from the current SOI platform.

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