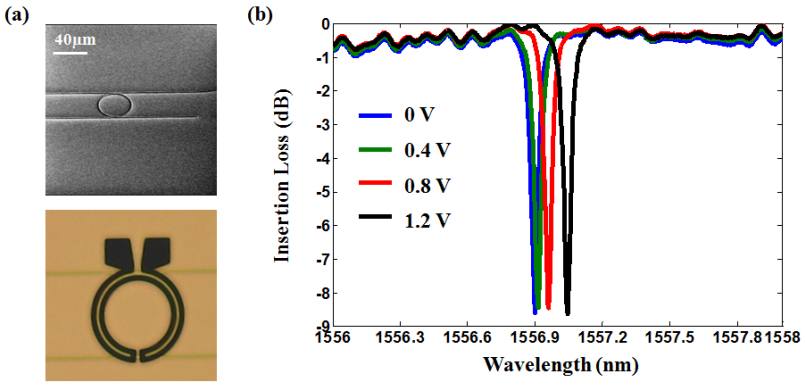

Fig. 5. (a) The SEM (top) and microscope (bottom) images of the micro-ring; (b) Transmission spectrum under different bias-voltage.

Table 2. Performance Benchmarking with State-of-the-art Multi-layer Platforms

Group	Optical Layer 1 (OL2)	Optical Layer 2 (OL1)	OL2 waveguide loss	Inter-layer loss (per transition)	Active integration
[4]	400nm PECVD Si_3N_4	400nm PECVD Si_3N_4	1dB/cm @1580nm	N.A.	No
[5]	100nm LPCVD Si_3N_4	500nm Si	1.2dB/m @1590nm	>0.4dB	No
[6]	3μm SiO_x	200nm Si	0.57dB/cm @1550nm	<0.37dB	Si VOA
[7]	400nm LPCVD Si_3N_4	220nm Si	N.A.	0.5dB	Ge PD
This work	600nm PECVD Si_3N_4	220nm Si	0.8dB/cm @1580nm 0.24dB/cm @1270nm	<0.2dB	Heater

5. Conclusions

In summary, we presented the fabrication and characterization of a CMOS-compatible Si_3N_4–on-SOI platform using a back-end approach. By suppressing the scattering loss, 0.8 dB/cm propagation loss is achieved with a 600nm-height PECVD Si_3N_4 waveguide at λ = 1580nm. An inter-layer transition coupler is designed on the platform. Ultra-low transition loss of < 0.2dB/transition is measured over 70nm-bandwidth, which is the lowest loss among all reported inter-layer transition coupler. We have also characterized the platform for O-band operation, with 0.24dB/cm propagation loss and 0.2dB/transition ILTL. Furthermore, a thermally tuned micro-ring filter is demonstrated on the platform, with Q > 30,000, insertion loss < 1dB, and thermal tuning efficiency of 0.11nm/mW. These preliminary results validate the feasibility and capability of the presented platform to further advance silicon photonics technology from the current SOI platform.

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