Three-dimensional (3D) monolithically integrated photodetector and WDM receiver based on bulk silicon wafer

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Abstract: We propose a novel three-dimensional (3D) monolithic optoelectronic integration platform. Such platform integrates both electrical and photonic devices in a bulk silicon wafer, which eliminates the high-cost silicon-on-insulator (SOI) wafer and is more suitable for process requirements of electronic and photonic integrated circuits (ICs). For proof-of-concept, we demonstrate a three-dimensional photodetector and WDM receiver system. The Ge is grown on a 8-inch bulk silicon wafer while the optical waveguide is defined in a SiN layer which is deposited on top of it, with ~4 μm oxide sandwiched in between. The light is directed to the Ge photodetector from the SiN waveguide vertically by using grating coupler with a Aluminum mirror on top of it. The measured photodetector responsivity is ~0.2 A/W and the 3-dB bandwidth is ~2 GHz. Using such vertical-coupled photodetector, we demonstrated an 8-channel receiver by integrating a 1 × 8 arrayed waveguide grating (AWG). High-quality optical signal detection with up to 10 Gbit/s data rate is demonstrated, suggesting a 80 Gbit/s throughput. Such receiver can be applied to on-chip optical interconnect, DRAM interface, and telecommunication systems.

OCIS codes: (130.0250) Optoelectronics; (130.3120) Integrated optics devices; (040.5160) Photodetectors; (050.2770) Gratings.

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1. Introduction

Silicon-based optoelectronic integrated circuits using CMOS technology have attracted great attention with rapid development in the past decade [1–5]. Silicon based opto-electric integrated circuit (Si-OEIC) is potentially with wide applications in long haul communications, fiber-to-the-home (FTTH), very short reach optical interconnect, and the on-chip optical interconnection. Many silicon photonic device building blocks have been investigated and demonstrated, e.g., WDM MUX/DEMUX [6–8], thermal-optical switches [9–11], high-speed optical modulators [12–15], and Ge-on-silicon photodetector (PD)

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[16,17]. Optical circuit blocks are also demonstrated, e.g., optical cross connect (OXC) [18,19], wavelength selective switch (WSS) [20,21], and optical transceiver [22–25].

At present, most of the Si-OEIC devices are based on silicon-on-insulator (SOI) technology due to the high index contrast between silicon and silicon dioxide for very good optical confinement, which results in 100 and even 1000 times reduction in device footprint. However, SOI is with 10 times higher cost comparing to bulk silicon wafers, and most of the electronic integrated circuits (ICs) are still made on bulk-Si substrate. Even for those optical and electrical IC building up on SOI, the SOI technology still faces other issues. For instance, while the optical devices require thick buried oxide (BOX) for reduced evanescent wave loss, the electrical devices requires thin BOX for thermal dissipation to silicon substrate.

In order to overcome these, we propose a three-dimensional (3D) monolithically integrated OEIC platform. Such OEIC platform is based on bulk silicon wafer. The electronic devices are defined in the silicon substrate, whereas the optical devices are fabricated in deposited materials on top of it. A low index layer, such as silicon dioxide, is sandwiched in between them as insulating or optical cladding layer. Compare the price difference between SOI wafer and bulk silicon wafer, additional cost from few steps of deposition process can be ignored. Besides the aforementioned advantages of cost and BOX issue, such 3D-OEIC platform has some other advantages: 1) The optical devices are made by the low-index material layer. For most of the CMOS compatible materials, lower index materials is typically with lower thermal optical coefficient, as result, it is less sensitive to the temperature, and meanwhile, it is of lower polarization independence. 2) A large wavelength range can be selected for optical devices, which is an advantage comparing to the SOI devices with optical wavelength longer than 1.1 μm. 3) Materials with higher non-linearity can be adopted. Thus, some other functional optical devices with niche application can be realized, such as nonreciprocal device, Raman applier, four wave mixing devices, etc [26–28].

As a proof-of-concept demonstration, we show a 3D monolithically integrated photodetector system. The Ge photodetector is built up directly on top of a bulk silicon wafer, while the optical waveguide is formed in the subsequently deposited SiN layer. The insulation oxide layer is ~4 μm to distance both devices. The optical light coupling between the waveguide and the Ge photodetector is through a vertical coupling scheme combining a grating coupler with an Al mirror on top. Optical receiver is also demonstrated with up to 80 Gbit/s data transmission by integrating such 3D photodetectors and a 1 × 8 AWG at telecommunication wavelength.

2. Device design, fabrication, and characterization

2.1 Device design

Figure 1(a) shows the schematic of the evanescent coupled Ge photodetector in SOI platform. The optical waveguide is defined in the Si layer with the Ge PD grown on top of the Si layer. In this case, the optical coupling is realized by evanescent coupling between Si waveguide and Ge layer. Figure 1(b) shows the schematic of the proposed 3D photodetector system in a bulk Si platform. The Ge layer is blankly or selectively grown on the silicon substrate, while the optical waveguide layer is deposited on top of it with low index material interlayer in between for separation. In general, the interlayer material can be oxide, while the optical waveguide layer could be polymer, SiN, SiON, or other higher index material. The optical light is coupled into the Ge layer by using a vertical grating coupler with a metal mirror on top of it to enhance the light collection. Similar concept of using the grating coupler with metal mirror's function was proposed and discussed in the context of fiber coupling scheme by Zaoui et al. [29]. So in theory, similar improvement would be expected in our approach with the mirror to reflect down the light.

#211017 - $15.00 USD Received 28 Apr 2014; revised 27 Jun 2014; accepted 29 Jun 2014; published 5 Aug 2014

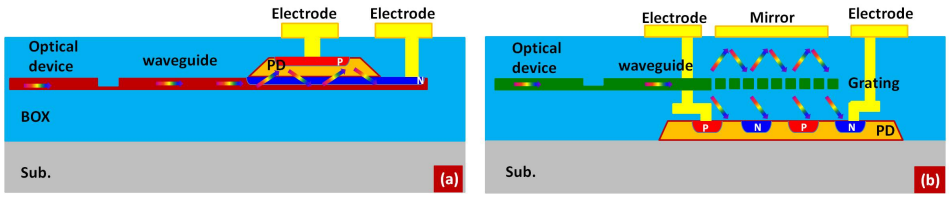

Fig. 1. Schematic illustrations for (a) the SOI-based photodetector, and (b) the proposed bulk Si-based photodetector system.

In the current demonstration, we adopt the SiN channel waveguides with 400 nm in height and 1 μm in width. The refractive index is 2 [30]. In order to monitor the input power to the Ge PD, we design Y-branch structure to split the input light, which is schematically shown in Fig. 2(a). One of the outputs is directed to the 3D photodetector, while another output is a straight waveguide with inverse taper for easy fiber/waveguide coupling. The waveguide is adiabatically taped from 1 μm to 400 nm. The taper length is 300 μm. The Ge photodetector sits beneath the SiN waveguide with a lateral P-i-N structure. The implantation regions for P and N are interleaved with 1 μm un-doped intrinsic region in between, as shown in Fig. 2(b). In order to increase the light coupling to the Ge photodetector, SiN vertical grating coupler is designed on top of the Ge region. In addition, an Al mirror layer on top of the grating coupler is designed in order to enhance the light collection. The design of the grating coupler is schematically shown in Fig. 2(c). The curved grating is with an ellipse shape [31] and with period of 1.1 μm.

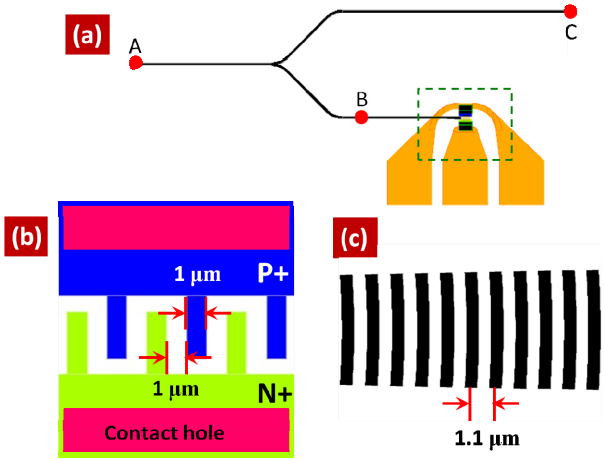

Fig. 2. (a) Design of the Y-branch integrated with the 3D photodetector with vertical coupler for light coupling. (b) The interleaved P-i-N structure. (c) The design of the curved grating.

2.2 Fabrications

We start the fabrication process from an 8-inch bulk silicon wafer. Firstly the wafer is pre-cleaned, followed with the growth of 1 μm germanium blankly. In order to increase the electrical field in the intrinsic Ge region to increase PD response speed, we etch away the P + and N + regions with 400 nm steps, followed by the P + and N + implantations separately. The implantations ensure the doping of the implants into the sidewall with 30 degree tilting angle and 90 degree rotation angles repeating for four times. In order to attain uniform doping concentrations in the Ge side wall, two steps implantations with different energies and doses are used for both P + and N + implantations with dosage of 4×10^{15} cm^{-2}. A 1 μm intrinsic region is designed between the P + and N + regions to increase the light collection area. After annealing at 500° for 30 sec, 400 nm SiO_2 layer is deposited, followed with contact holes opening. A metal film of 25 nm TaN/750 nm AlSiCu/50 nm TaN is deposited and etched as

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the first metal contact layer. Another 4.5 μm oxide layer is deposited to clad the Ge and metal layers, followed by reverse etching and chemical-mechanical planarization (CMP) to smooth the surface. After that, a 400 nm SiN layer is deposited by low-temperature PECVD for the optical waveguide. After the formation of SiN waveguide, another 3.4 μm SiO_2 is deposited on the SiN waveguide layer, followed with second reverse etching and CMP. After the definition of the via holes to the first metal layer, the second metal layer with 25 nm TaN and 2 μm AlSiCu is deposited and patterned. This layer is used for both electrical contact pad and the reflection mirror. Finally, the deep trench is defined in order for fiber edge coupling with waveguide. Figure 3(a) shows the microscope image of the top view, in which the contact metal to P + and N + implantation areas and the metal mirror are labeled. Figure 3(b) shows the cross-sectional TEM image of the Ge region, illustrating the P-i-N junctions with shallow etch in the P and N regions, the vertical grating coupler, and the Al mirror. Figure 3(c) shows the SEM of the curved grating coupler in SiN layer.

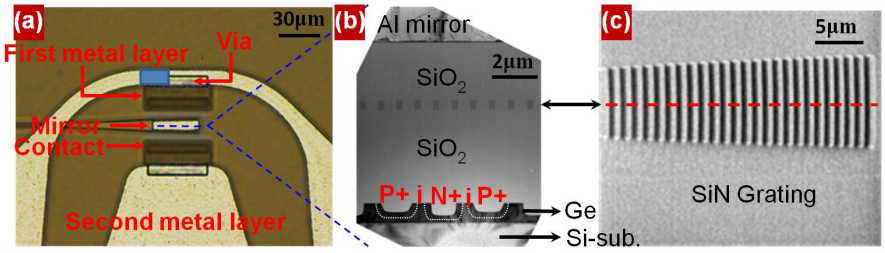

Fig. 3. (a) Optical microscope image of the fabricated device. (b) The cross-sectional TEM image of the Ge PD region. (c) The SEM of the SiN grating coupler.

2.3 Testing results and discussion

2.3.1 Static characteristics

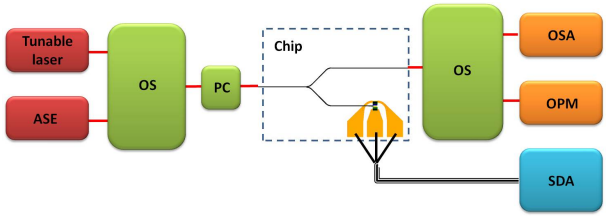

Fig. 4. Characterization setup for the static performance testing. OS: optical switch. PC: polarization controller. OSA: optical spectrum analyzer. PM: Power meter. SDA: semiconductor devices analyzer.

Firstly, we characterize the photodetector static performances regarding to the optical loss, current-voltage properties, and the responsivity. The testing setup is shown in Fig. 4. A tunable laser and a wideband ASE source are connected to an optical switch for the light source selection, followed with a polarization controller (PC, Agilent 8169A) to control the light to be TE-polarized. The output light is coupled into the silicon chip through a single-mode polarization-maintenance fiber. The light output from the optical branch of the Y-splitter is coupled to a single-mode lensed fiber and finally directed to another optical switch, which can switch the output light either to an optical power meter (OPM, Newport 2832C) for power reading or an optical spectrum analyzer (OSA, Ando AQ6317B) for spectrum measurement. The light that goes to another branch of the Y-splitter is detected by the photodetector, and the photocurrent is measured by a semiconductor device analyzer (SDA, Agilent B1500).

We firstly studied the SiN waveguide loss using cut-back structures. The waveguide insertion loss with different lengths is measured by ASE light source and OSA. The TE-mode

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waveguide propagation loss as a function of the wavelength is shown in Fig. 5(a). The minimal loss at L-band is ~1 dB/cm, while it increases significantly in C-band and reaches to ~9 dB/cm at 1520 nm, which is due to the absorption of the Si-H and N-H bonds. The coupling loss is extrapolated using the transmission loss, which is shown in Fig. 5(b). The coupling loss is ~3.4 dB/facet. Similar to the waveguide cut-back technique, we use a 7-stage cascaded Y-branch to measure the Y-branch loss, as shown in Fig. 5(c). Thus, the Y-splitter excess loss is ~0.6 dB/junction. As shown in Fig. 5(b) and 5(c), both coupling loss and Y-branch losses are wavelength-independent.

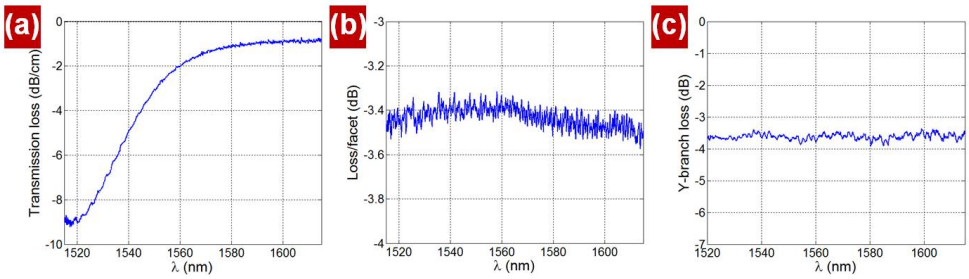

Fig. 5. Passive elements losses for TE mode. (a) Waveguide propagation loss. (b) Fiber/tapered waveguide coupling loss. (c) Y-branch loss.

Figure 6 shows the IV characteristics for the demonstrated 3D photodetectors with 28 μm and 60 μm length with and without light input. The calibrated input power is ~266 μW at 1550 nm. The dark currents for 28 μm and 60 μm long photodetectors are respectively ~0.87 μA, and ~2.12 μA. The relatively high dark current is due to the increased P-i-N diode length by adopting the interleaved structures. The photocurrent is relatively higher for the 60 μm long photodetector than that of 28 μm one. This suggests that the light absorption is stronger by using longer photodetector, possibly due to the more completed light scattering from the SiN grating to the underneath photodetector.

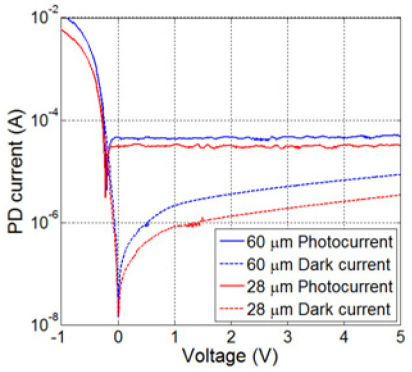

Fig. 6. The I-V characteristics for the 3D photodetectors with 28 μm (red) and 60 μm (blue) in length. Dished lines: without light input. Solid lines: with light input of ~266 μW.

The photodetector responsivity is measured by change the input optical powers. By measuring the output power from the reference branch, we can obtain the calibrated power that reaches to the grating/photodetector, by subtracting the coupling loss and waveguide loss. Figure 7(a) shows the measured photocurrents as functions of the input powers upon different bias voltages. The photo-responsivity is extracted by linearly fitting the measured curves, which is shown in Fig. 7(b), as function of bias voltage. The responsivity is between 0.2~0.22. It is smaller than that of ~0.7 - 0.9 [16] for conventional SOI waveguide photodetector, yet it's comparable with that of vertical coupled PD. Germanium absorption coefficient α is close to ~7000 cm^{-1}. For 1 μm thick germanium, ~50% light power is

#211017 - $15.00 USD Received 28 Apr 2014; revised 27 Jun 2014; accepted 29 Jun 2014; published 5 Aug 2014

absorbed. The germanium thickness must be larger than 3 μm in order to absorb ~90% light. Furthermore, if using the APD structure to replace current P-i-N structure [32], the sensitivity can be improved as high as 12 A/W.

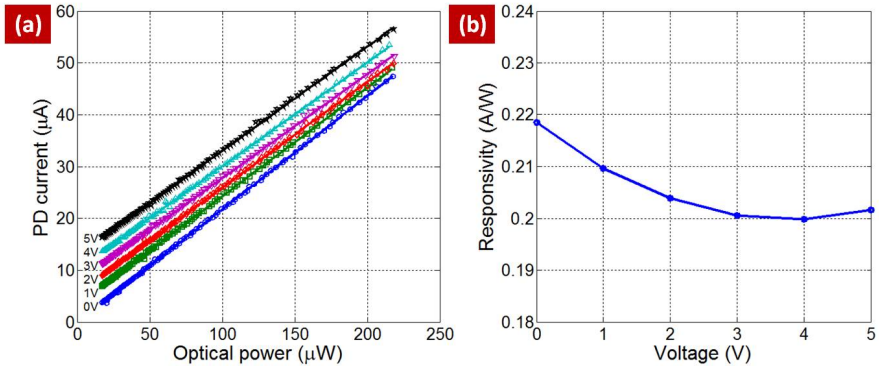

Fig. 7. (a) The photodetector responses upon the input power change at different bias voltages. The input light is at 1550 nm. (b) The extracted responsivity as functions of the reverse bias voltage.

2.3.2 Dynamic characteristics

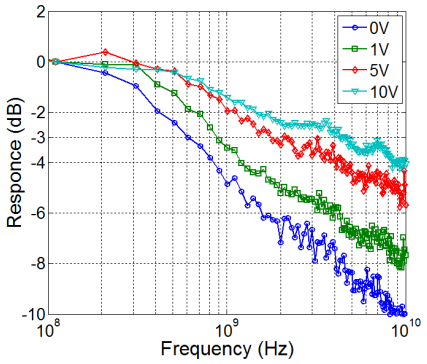

Fig. 8. Photodetector response for small signal. The bias voltages are 0V (blue), 5V (green) and 10 V (red) respectively.

For investigation of dynamic behavior of the 3D photodetector, we employed network analyzer (Agilent E8363C PNA Network Analyzer) to measure the small signal response. Figure 8 shows the measured S21 response under different reverse bias voltages. For reverse bias at 5 V, the 3-dB bandwidth is close to ~2 GHz. And at −10 V, it increases to ~4 GHz. We attribute to the relatively low bandwidth to the following two reasons. 1) The device shown in Fig. 8 is with implant region length of 60 μm, which corresponds to a junction area of ~180 μm × 0.5 μm. This makes larger capacitance. 2) The Ge slab thickness is ~0.5 μm, which makes electron field relatively lower, and causes the carriers with longer transit time in slab. However, such shortcomings can be improved by adopting vertical P-i-N structure.

In order to investigate the signal transmission, we send PRBS signal to the optical receiver and measure the electrical signal from the photodetector. Figure 9 shows the eye diagrams of the signal with data rates of 1 Gb/s, 2.5 Gb/s, 5 Gb/s, and 10 Gb/s at 5 V reverse bias, which show clear open eyes with high-quality signal detection.

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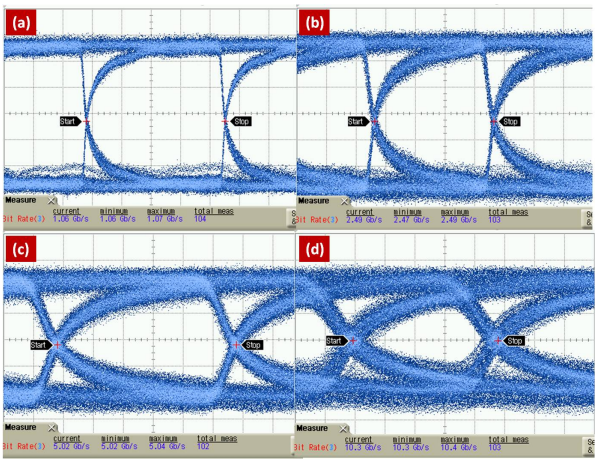

Fig. 9. The measured eye diagrams for the vertical PDs. (a)1 Gb/s, (b)2.5 Gb/s, (c)5 Gb/s and (d)10 Gb/s.

2.3.3 WDM integrated receiver

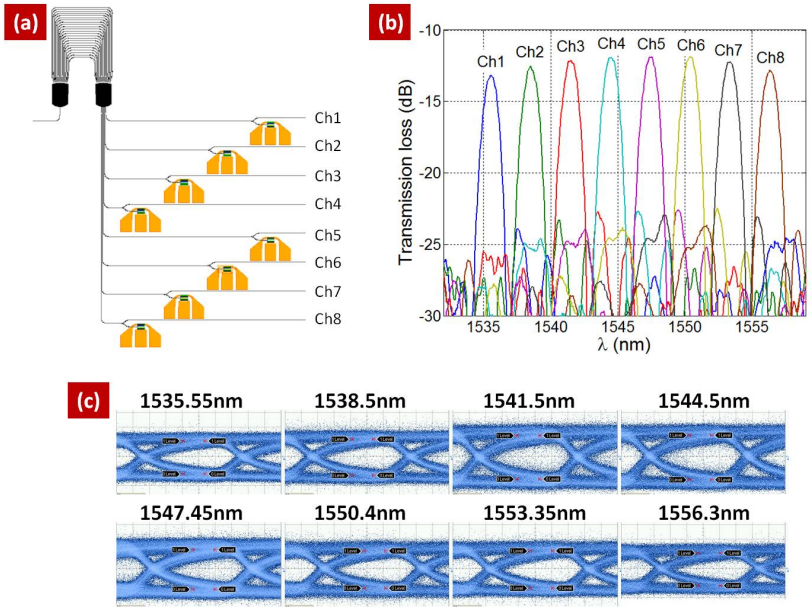

Fig. 10. Proof-of- principle demonstration of an 80 Gbit/s optical receiver. (a) The layout of the receiver integrating a 1 × 8 AWG and 3D photodetector. (b) The measured optical spectra of the AWG. (c) The measured electrical eye diagrams for the photodetectors.

As a proof-of-principle demonstration, we show here an optical receiver by monolithically integrate an 8-channel SiN AWG and 3D photodetector together. Figure 10(a) shows the design layout of such optical receiver. Each of the output of the AWG is also split into two branches with one reference arm for optical spectra measurement and the other branch integrating with the 3D photodetector. Figure 10(b) shows the measured optical transmission spectra of the 8-channel AWG. The transmission losses are 12 ~14 dB.

Figure 10(c) show the measured eye diagrams from each of the channel with 10 Gbit/s data rate. The open eye diagrams suggest the high-quality data transmission and detection with up to 80 Gbit/s capabilities.

#211017 - $15.00 USD Received 28 Apr 2014; revised 27 Jun 2014; accepted 29 Jun 2014; published 5 Aug 2014

3. Conclusion and outlook

In this work, we proposed a 3D monolithic OEIC integration platform based on bulk-silicon. This OEIC platform eliminates the use of high-cost SOI wafer. Consequently, the electronic circuit portions, including drivers for lasers or modulators, trans-impedance Amplifier (TIA) for photodetectors, electrical signal amplifiers, and dynamic random-access memory (DRAM) and alike can be fully leveraged and realized on same bulk-silicon wafer with the addition of photonic circuits. This is because the photonic devices can are fabricated on deposited materials via back-end of the line (BEOL) process as demonstrated in this work. Therefore, this platform fully utilizes the advantages from both electrical and optical while eliminates the need of SOI substrate.

As proof-of-concept, we demonstrate a 3D OEIC receiver. The waveguide coupled scattering grating was inserted between Al mirror and Ge P-i-N photodetector. The photodetector exhibits responsivity of ~0.2 A/W and the bit rate is measured to be up to 10 Gbit/s. Furthermore, with the function of a 1 × 8 WDM receive system with 3D PD integrated together, it suggests that 80 Gbit/s aggregated data rates can be obtained.

Acknowledgments

This work was supported by the Science and Engineering Research Council of A*STAR (Agency for Science, Technology and Research), Singapore, under SERC grant number 1021740174 and 1122804038. One of author is supported by National Natural Science Foundation of China (NSFC, Grant No. 61177090, 61377048).

#211017 - $15.00 USD Received 28 Apr 2014; revised 27 Jun 2014; accepted 29 Jun 2014; published 5 Aug 2014