

# Silicon Optical Interconnect Device Technologies for 40 Gb/s and Beyond

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(*Invited Paper*)

**Abstract**—Important active technologies, modulators, photodetectors, and thermo optics for low-energy silicon optical interconnects are discussed. High-speed performance up to 40 Gb/s is reported for the silicon modulators and germanium photodetectors, and approaches for further improvement in speed and efficiency are presented. Low-voltage avalanche multiplication is demonstrated, giving a gain-bandwidth product of 75 GHz, while the combined effects of multiplication gain and the Franz-Keldysh effect enable a 5-μm-long germanium photodetector to achieve responsivity in the L-band that is comparable to that in the C-band. With trench-based thermal isolation, a low switching power of 0.4 mW is achieved for a thermo optic switch.

**Index Terms**—Avalanche gain, Franz-Keldysh effect, germanium photodetectors, low-energy optical interconnects, silicon modulators, thermo optics.

## I. INTRODUCTION

THE aggressively increasing demand for bandwidth and low latency, driven by bandwidth consumers such as cloud computing, social networking, and high-definition multimedia content streaming, could change how future data centers are built. Silicon photonics, which is rapidly gaining attention for its potential to enable low-cost, high-bandwidth and highly integrated interconnect systems with exceedingly low-energy consumption, could play a vital role in future data centers. One of the key advantages of silicon photonics is the potential to integrate traditionally large footprint devices into ultracompact photonic integrated circuits (PICs) or systems on a chip at low cost. This could revolutionize how space is utilized in future data centers and could enable efficient implementation of emerging data center architectures such as that reported in [1], and pave the way for the future. Moreover, cooling requirements for such

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ultracompact PICs or systems would be radically different and is expected to offer dramatic energy savings.

In this paper, we will describe three key active silicon photonics device technologies that are vital to the silicon photonics integrated circuit platform. These are the silicon modulator, germanium photodetector, and integrated thermo optics, and will be described in three sections. This paper describes high-speed operation of silicon modulators and germanium photodetectors at up to 40 Gb/s and discusses techniques for obtaining higher speed and better efficiency.

For the silicon modulator, the main focus will be on the carrier depletion-mode silicon p-n junction modulator. This type of silicon modulators utilizes the free carrier dispersion effect to realize embedded phase shifters within a waveguide. In depletion-mode operation, the p-n junction depletion width is modulated by the applied voltage. By inserting such phase shifters into a Mach-Zehnder interferometer (MZI) configuration, broadband modulators for intensity [2]–[9] or phase modulation formats [10] can be realized. There have also been many reports of high-performance resonator-based modulators for improved modulation efficiency [11]–[19]. Often, this comes with the drawback of reduced spectral bandwidth and increased sensitivity to fabrication errors. In this paper, we will focus on depletion-mode p-n junction phase shifters in general, using the Mach-Zehnder modulator as a simple test vehicle for investigations. We also describe loss reduction and efficiency improvement techniques. It should be noted that these techniques are also relevant and can be applied to resonator-based modulators using depletion-mode phase shifters.

For the germanium photodetector, we will focus on the photodetector in a waveguide coupling configuration. It is without doubt that the same fabrication process can be used to fabricate normal-incidence photodetectors, but waveguide photodetectors enable chip scale circuit integration. The waveguide germanium photodetector also has superior long wavelength responsivity compared to normal-incidence photodetectors. We examine approaches relating to how the photodetector can be improved to indirectly reduce overall power consumption in the interconnect system, based on the premise of improving receiver sensitivity by the use of carrier multiplication gain.

Thermo optics is an important complement to electrooptics for phase tuning as they allow tuning in the opposite polarity. The optical loss due to free carrier absorption is also avoided. However, the use of multiple thermo optic devices on a silicon PIC can create power dissipation problems and can also lead to

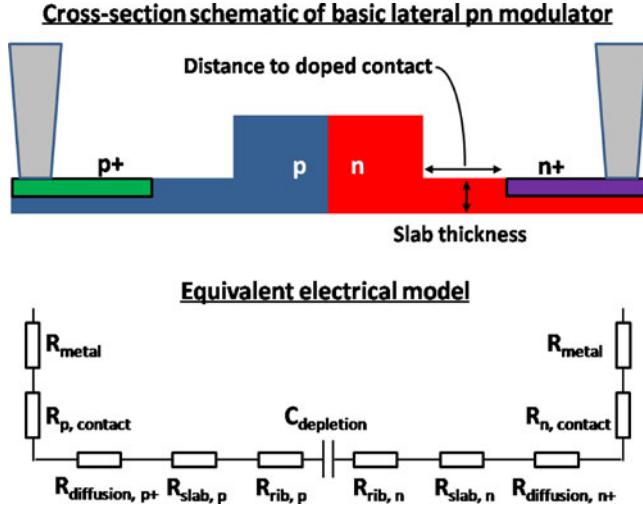


Fig. 1. Schematic of the basic LPN junction depletion-mode modulator phase shifter and its simplified equivalent electrical model.

thermal crosstalk issues. We discuss the approach of utilizing thermal isolation based on isotropic trench etching to improve the power efficiency.

## II. HIGH-PERFORMANCE SILICON MODULATORS

### A. Speed Improvement by RC Reduction

The speed (or bandwidth) of depletion-mode p-n junction silicon modulators is primarily limited by RC. Improving the speed itself can be a matter of decreasing  $R$  while maintaining a reasonable  $C$ , if one adopts a somewhat brute-force approach. Typically, this can be done by increasing the phase shifter doping, which reduces  $R$ , and by intentionally designing a gap between p and n phase shifter implant masks to ensure that the resultant junction doping concentration is not too high, so as to maintain a reasonable  $C$ . The drawback with doing this is that the speed often comes with an optical loss penalty due to increased free carrier absorption loss. Before going down this route, there is often room for speed improvement by simple optimization of the critical parameters.

The fabrication process and basic device structure are similar to that described previously in [20]. Fig. 1 shows the schematic of the basic lateral p-n (LPN) junction phase shifter and its simplified equivalent electrical model. The model is not meant to be an accurate representation but is instead intended to show the constituents of the series resistances. With optimization of the phase shifter's critical parameters (e.g., slab thickness, doped contact to waveguide distance, and metal RF electrode (coplanar waveguide) thickness/width), the parasitic resistances can be reduced, thereby reducing the total resistance  $R$ . By utilizing suitable test structures to determine the optimum parameters [20], the reduction of parasitic resistances can be achieved without adversely impacting other performance metrics such as optical loss or phase-shifting efficiency. Using this approach, an optimized version of the modulator reported in [20] was fabricated and tested.  $R_{\text{metal}}$  was improved by increasing the top metal thickness from 0.75 to 2  $\mu\text{m}$ , which also had the benefit

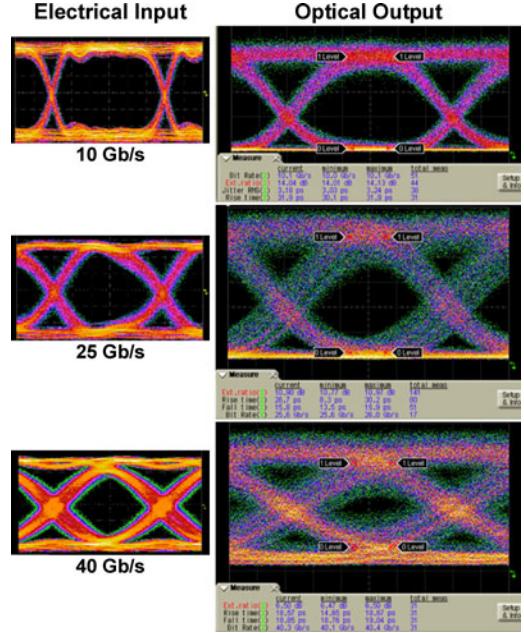


Fig. 2. Electrical input and optical output eye patterns. Extinction ratios of 14.0, 10.9, and 6.5 dB were obtained at 10, 25, and 40 Gb/s, respectively.

of reducing the coplanar waveguide's RF loss. It was found that a major contributor to series resistance was  $R_{\text{slab}}$ , which was addressed by increasing slab thickness, while monitoring optical loss to ensure minimal optical loss tradeoff. We managed to achieve higher modulation speed ( $f_{-3 \text{ dB}} = \sim 20 \text{ GHz}$ ), while maintaining the optical loss and phase-shifting efficiency as previously reported. Fig. 2 shows the electrical input and optical output eye patterns of the optimized MZI modulator at 10, 25, and 40 Gb/s. The phase shifters are 4 mm long and only one arm was driven in a single-ended manner ( $V_{\text{p-p}} = 6.5 \text{ V}$ ). The eye remains open at up to 40 Gb/s, albeit with a reduced extinction ratio. Extinction ratios of 14.0, 10.9, and 6.5 dB were measured at 10, 25, and 40 Gb/s, respectively. If the modulator's arms are differentially driven, the driving voltage can ideally be halved.

There is certainly room for improvement with regards to operation at high speeds, especially at 40 Gb/s. While the series resistance can still be further optimized to improve the p-n junction's RC limitation on overall bandwidth, obtaining a high-quality eye pattern at 40 Gb/s will also require the RF electrodes (electrical coplanar waveguides) to be improved. The relatively long length of the phase shifter (4 mm) necessitates at least equally long electrical coplanar waveguides. This creates two challenges.

The first challenge lies with obtaining good velocity matching between optical and electrical signals (in other words, realizing traveling wave electrodes), which is essential for obtaining a high-quality eye pattern with low jitter and large extinction ratio at 40 Gb/s and beyond. While TCAD software helps immensely with designing traveling wave electrodes, discrepancies between the modeled structure and the actual fabricated structure make it challenging to achieve perfect velocity matching. Moreover, since the distributed p-n junction forms part of the traveling wave electrode, the biasing voltage applied to the phase shifter also

affects the depletion capacitance and, hence, the electrical signal velocity. This basically means that perfect velocity matching can only be achieved at a particular bias voltage. That said, this is perhaps only academic and should likely have only minimal impact provided the bias voltage stays within a reasonable range.

The other challenge is with the significant RF propagation loss of RF electrodes [21] fabricated using CMOS-compatible metallization, which involves relatively thin metal layers. Using thin metal layers for the RF coplanar waveguide results in a large interaction with the noninsulating semiconductor substrate (i.e., Si). Using silicon-on-insulator (SOI) wafers with high resistivity handle wafers helps significantly to reduce this RF loss component, but the fact remains that if the phase shifters have to be long, the RF propagation loss becomes increasingly a constraint when we scale the operation speed to 40 Gb/s and beyond.

A simple and practical approach for overall improvement would be to reduce the length of the phase shifters. The shorter the length of the phase shifters, the more it obviates the need for perfectly velocity-matched traveling wave electrodes. Total RF loss would also decrease, naturally, because the RF coplanar waveguides will be shorter. Of course, simply reducing the length of the phase shifters will bring about drawbacks in itself. In the next two sections, we will describe two approaches that can help enable length reduction of the phase shifters while maintaining other aspects of the modulator's performance.

### B. Optical Loss Reduction by Doping Compensation

The doping concentration in the rib region simultaneously affects the modulation efficiency as well as the loss per unit length of the waveguide phase shifter. When the doping concentration levels are tuned, there is often a tradeoff between the modulation efficiency and the optical loss, making it difficult to reduce the optical loss without detrimental effects on the modulation efficiency. Next, we examine how the optical loss of the modulator phase shifter can be reduced by using a novel doping compensation technique [22], [23]. The technique works on the premise that the active region (i.e., region of free carrier modulation) of the phase shifter is actually confined in a narrow region in the center of the rib waveguide. The regions outside of that active region serve mainly to act as electrical contacts to the active region. However, there are less critical regions located near to the upper corners of the rib waveguide which do not significantly act as electrical contacts and yet still contribute to free carrier absorption loss. The idea is then to reduce the doping concentration in these less critical regions. The doping compensation technique is essentially a counterdoping process technique in which the doping concentration in these less critical regions can be reduced while minimizing impact on the active region itself.

Fig. 3 shows the process flow schematics which illustrate the difference in process steps between the baseline process flow and the doping compensation process flow. It can be seen that the doping compensation process simply involves two additional ion implantation steps before the waveguide etch process.

Fig. 4(a) and (b) plots the optical loss and the phase-shift efficiency ( $V_\pi \cdot L_\pi$ ) against the uncompensated width ( $W_P$  or

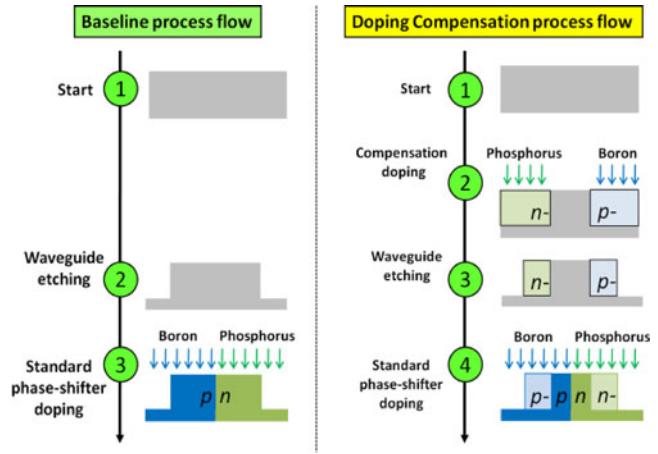


Fig. 3. Process flow schematics showing the difference in process steps between the baseline process flow and the doping compensation process flow.

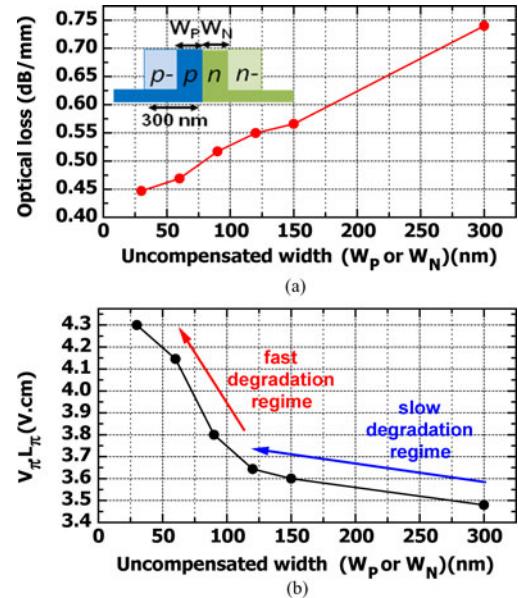


Fig. 4. Plot of (a) optical loss and (b)  $V_\pi \cdot L_\pi$  against uncompensated width ( $W_P$  or  $W_N$ , where  $W_P = W_N$ ).

$W_N$ ), respectively. In this case,  $W_P$  is designed to be the same as  $W_N$ . From Fig. 4(a), it is clear that the optical loss indeed decreases with an increasing degree of compensation (decreasing uncompensated width). However, it is important to examine the tradeoff in phase-shift efficiency plotted in Fig. 4(b). It is observed that the phase-shift efficiency does not degrade much at values of uncompensated widths above 120 nm (slow degradation regime). Below that, it progresses into a rapid degradation regime in which the phase-shift efficiency degrades rapidly with decreasing uncompensated width. Since the implantation masks rely on lithographic alignment, the transition point to fast degradation depends partially on the layer-to-layer registration. It is also expected that the compensating dopants will also diffuse horizontally. As the uncompensated width decreases, more compensating dopants diffuse into the active region, thereby reducing the effective doping concentration there. Hence, it is advisable to adopt a suitable value of uncompensated width

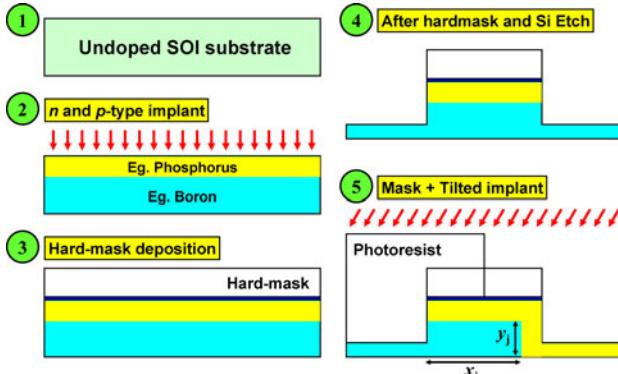


Fig. 5. Process flow schematics showing the difference in process steps between the baseline process flow and the doping compensation process flow.

that lies within the slow degradation regime to provide good fabrication process tolerance. To delay the transition point to the fast degradation regime, it would be necessary to reduce horizontal dopant diffusion by optimizing the rapid thermal anneal conditions. It is likely that a faster ramp rate to reduce transient enhanced diffusion and a lower peak temperature to reduce diffusion at the peak temperature would be beneficial. There would also be the concern that the speed of the device would be decreased when the uncompensated width is too small due to increased series resistance. Frequency response measurements confirm that even at an aggressive uncompensated width of only 90 nm, the bandwidth of the device is not degraded.

### C. Efficiency Improvement by Doping Design Changes

For submicrometer single-mode Si waveguides, it is typical to design waveguides with a low height-to-width aspect ratio. Due to this low height-to-width aspect ratio, it is expected that a phase shifter employing a vertical p-n (VPN) junction will have a higher overlap between the active modulation region and the optical mode, compared to a phase shifter employing an LPN junction. Indeed, modulators employing a VPN junction in low height-to-width aspect ratio submicrometer waveguides have been reported to have better phase-shift efficiency than those employing an LPN junction [24], [25].

We fabricated a modulator with a dominantly VPN junction using a modified process integration flow that is compatible with our baseline silicon photonics process flow. Fig. 5 shows the schematic of the process flow. First, a window is patterned to expose the phase shifter region for implant. Both n- and p-type dopants are implanted into this window but to different target depths. In this study, n-type dopants (Phosphorus) were targeted to a shallower depth, whereas p-type dopants (Boron) were targeted to a deeper depth. Tuning the implantation energies and doses in this step will determine the vertical doping profile and junction location. Next, the waveguide is patterned and etched using a hard mask scheme, which is similar to the conventional process flow we use for rib waveguide formation. In the conventional process flow, the hard mask will then be removed using dilute hydrofluoric acid. In this process flow, the hard mask is left intact to serve as an implantation mask. At

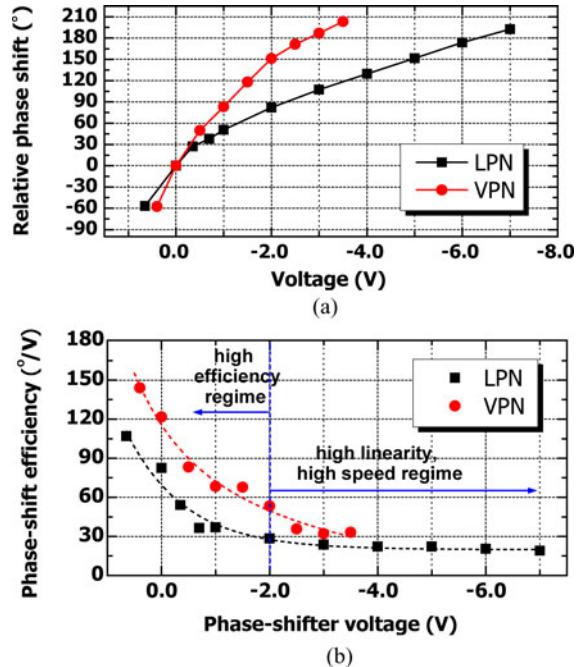


Fig. 6. Plot of (a) relative phase shift and (b) phase-shift efficiency against phase shifter voltage. Phase shifters are 4 mm long.

this point in the process, it can be seen that the slab regions are currently doped p-type. In the next implantation step, a photoresist mask is patterned to expose one side of the rib waveguide for implantation. A tilted-angle implant is then performed to implant n-type dopants into the side of the rib waveguide and to counterdope the slab region back to n-type. The final highly doped contact implants are not shown in the schematic but are done in the exact same way as those for the LPN junction. The advantage of fabricating the phase shifter using such a process is that the VPN junction location ( $y_j$ ) and the LPN junction location ( $x_j$ ) are both determined by ion implantation processes, allowing for accurate and repeatable junction locations (of the order of several nanometers). In comparison, in the conventional LPN junction phase shifter, the LPN junction location is determined by lithographic alignment, which is subject to a larger variation (of the order of several tens of nanometers).

Fig. 6(a) plots the relative phase shift of the VPN junction phase shifter and the LPN junction (LPN) phase shifter against bias voltage. A relative phase shift of  $180^\circ$  ( $\pi$  rad) is achieved at a voltage of 6.4 V for the LPN junction phase shifter and at 2.8 V for the VPN junction phase shifter. Since both phase shifters have identical lengths of 4 mm, this gives a  $V_\pi \cdot L_\pi$  value of 2.56 and 1.12 V·cm for the LPN and VPN junction phase-shifters, respectively. It is clear that the VPN junction phase shifter is more efficient. The  $V_\pi \cdot L_\pi$  value is also consistent with that reported in [24] and [25]. Fig. 6(b) plots the phase-shift efficiency in  $^\circ/\text{V}$  against the phase shifter voltage. It can be clearly observed that the phase-shift efficiency increases as we progress to lower phase shifter voltages, be it for the LPN or the VPN junction phase shifter. Operating in this high-efficiency regime would allow us to drive a depletion-mode MZI modulator using a low-voltage CMOS driver, since the efficiency is roughly

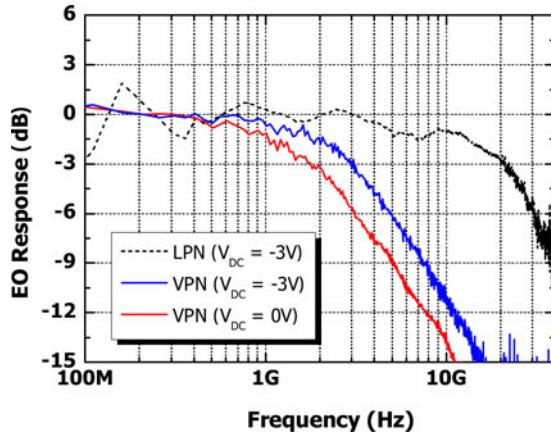


Fig. 7. EO frequency response of a LPN modulator at a bias voltage of  $-3\text{ V}$  and a VPN modulator at bias voltages of  $0$  and  $-3\text{ V}$ .

tripled. On a side note, operating in the high-bias-voltage regime can be beneficial for analog applications where high linearity is desirable.

Total power consumption comprises static and dynamic components. If the modulator is biased at a negative voltage, there will be significant static current flowing into the termination resistor leading to Joule heating losses. As an example, with a  $50\text{-}\Omega$  termination resistor, this would incur a power consumption of  $180\text{ mW}$  for a bias voltage of  $-3\text{ V}$ . One possible solution would be to use capacitive coupling (ac coupling) to the termination resistor, but will then require relatively large capacitors and additional design complexity. Hence, operating at zero bias would offer an additional advantage in this regard since the termination resistor can be dc coupled. On the electrode's input end, the bias tee for combining dc and the RF signal can also be eliminated.

Fig. 7 shows the frequency response of the MZI modulator with LPN and VPN junction phase shifters. At a similar dc bias voltage of  $-3\text{ V}$ , it is observed that the bandwidth of the VPN junction MZI modulator is much lower than that of the LPN junction MZI modulator due to RC. The extracted series resistance of the VPN junction phase shifter is approximately four times that of the LPN junction phase shifter. The capacitance was also measured to be  $\sim 1.9$  times that of the LPN junction phase shifter. The cause of the high series resistance was determined to be due to an overly thin slab that forms the lateral electrical contacts to the junction. The focus of the discussion is not on the comparison between the VPN and the LPN modulators' bandwidths, given that the VPN modulator is comparatively unoptimized in terms of series resistance unlike the LPN modulator. Instead, it is important to observe that operating the VPN junction modulator at zero bias results in a bandwidth penalty tradeoff compared to operating at  $-3\text{ V}$ . This is expected since the depletion capacitance at zero bias is higher than that at  $-3\text{ V}$ . It is fortunate, however, that this bandwidth penalty can be traded off against additional free carrier absorption optical loss by doping the slab regions to a higher doping concentration for reduced series resistance.

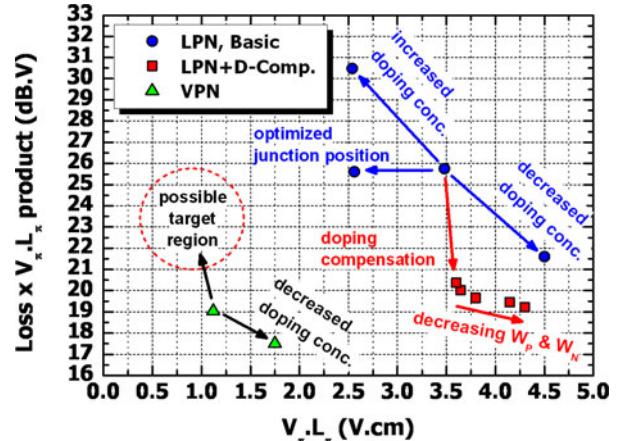


Fig. 8. Plot of the  $(\text{Loss} \times V_\pi \cdot L_\pi)$  product as an FOM against  $V_\pi \cdot L_\pi$  of the various modulator phase shifter types.

It is important to be able to assess and evaluate the overall performance of the different modulator phase shifter types. The product of the normalized optical loss (in dB/cm) and the  $V_\pi \cdot L_\pi$  can be used as a figure-of-merit (FOM) which helps in the assessment of a modulator's loss-to-efficiency tradeoff. (Note that the optical loss refers to the phase shifter loss and excludes optical coupling loss.) A lower value means that the modulator will have a lower absolute phase shifter optical loss for a phase shifter which is long enough to satisfy a given  $V_\pi$  specification. Fig. 8 plots the loss  $\times V_\pi \cdot L_\pi$  FOM against  $V_\pi \cdot L_\pi$ . It is desirable for the modulator to have a low loss  $\times V_\pi \cdot L_\pi$  FOM value as well as a low  $V_\pi \cdot L_\pi$ . This essentially indicates that the modulator can have a smaller footprint, higher efficiency, and lower optical loss. On the graph, this means that it is desirable to move leftward and downward. One limitation to note is that RF bandwidth information is not represented in this plot and has to be assessed separately.

We can start by looking at the basic LPN modulator in Fig. 8. It can be seen that simply increasing the doping concentration to decrease (improve) the  $V_\pi \cdot L_\pi$  results in a higher loss  $\times V_\pi \cdot L_\pi$  FOM. This indicates that despite the fact that the phase shifters can be shortened as a result of the improved efficiency, its absolute optical loss will increase. On the other hand, simply decreasing the doping concentration will improve the FOM but is at the expense of  $V_\pi \cdot L_\pi$ . Furthermore, having longer phase shifters is something to avoid since long RF electrodes will have high loss and will be difficult to velocity match. By using the doping compensation approach described in Section II-B, it can be clearly observed in Fig. 8 that optical loss is reduced without compromising  $V_\pi \cdot L_\pi$ . It also shows that doping compensation need not be too aggressive as the returns are rapidly diminishing due to counterdopants diffusing into the active region. The VPN modulator has the best FOM and lowest  $V_\pi \cdot L_\pi$ . However, this plot does not show the VPN's modulator tradeoff, which is the reduced bandwidth. The series resistance can be reduced by introducing additional doping of the intermediate slab regions between the highly doped contacts and the waveguide rib. The additionally doped slab regions, though not having strong overlap with the bulk of the optical mode that is confined within the

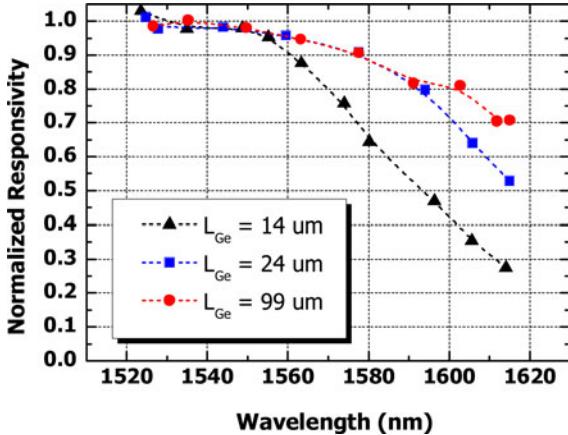


Fig. 9. Normalized spectral responsivity for photodetectors of different lengths (photodetectors are biased at  $-1 \text{ V}$ ).

rib, will still result in some additional optical loss. Despite trading off the optical loss, it is likely that the VPN modulator will still have a lower loss than the LPN modulator, while having a better  $V_\pi \cdot L_\pi$ , and is the subject of further investigation.

### III. HIGH-PERFORMANCE WAVEGUIDE GERMANIUM PHOTODETECTORS

#### A. Speed Improvement by RC Reduction

In [20], we investigated the differences between lateral and vertical photodetector structures and the impact of post-epitaxy annealing on the device performance. In this study, we focus on improving vertical photodetectors in which the epitaxial Ge thickness is  $\sim 850 \text{ nm}$ .

The bandwidth of a p-i-n Ge photodetector can be limited by carrier transit time or RC [26]. From a design perspective, it may be desirable to maintain a thin enough intrinsic Ge layer thickness (such that the carrier transit time is short), so that the bandwidth is limited mainly by RC. In this RC-limited regime, the bandwidth of the photodetector can then be scaled upward by scaling the area of the p-i-n junction downward, since this effectively scales down the capacitance.

An obvious way to do this in a waveguide Ge photodetector would be to reduce the length of the p-i-n junction (photodetection region). However, there are tradeoffs associated with length reduction. Ge has an absorption coefficient which rolls off rapidly beyond 1550 nm [27]. While it is possible to extend the rolloff point toward the longer wavelengths using strain-induced band structure modifications or materials engineering, the processes to achieve these are still not mature. Fig. 9 shows the normalized spectral responsivity for photodetectors of different lengths. All the photodetectors achieve absolute responsivities of  $\sim 0.9 \text{ A/W}$  at wavelengths below 1550 nm. For the photodetector with a length of  $14 \mu\text{m}$ , there is a sharp rolloff in responsivity beyond about 1555 nm. This can be attributed to the insufficient length of the Ge absorption region which results in incomplete absorption of light at longer wavelengths. The photodetector with a length of  $100 \mu\text{m}$  is clearly long enough to absorb most of the light even beyond 1600 nm. It should

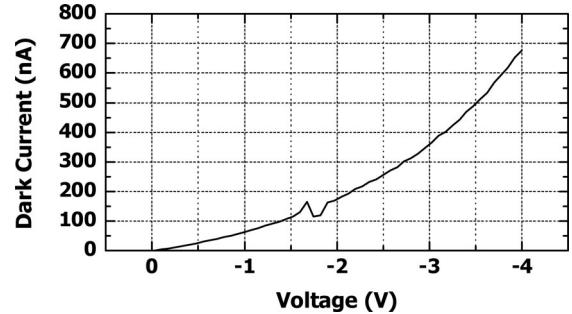


Fig. 10. Dark current of  $24\text{-}\mu\text{m}$ -long photodetector at different reverse bias voltages.

be noted that the gradual rolloff in responsivity observed is not entirely due to incomplete absorption. Instead, this is also due to optical losses in the waveguide photodetection region as a result of scattering losses as well as optical absorption losses which do not contribute to the photocurrent. The absorption losses are induced by modal overlap with the metal electrodes and highly doped contact regions of the p-i-n junction. On this subject, others have reported improvements in responsivity by laterally offsetting the metal from the center of the absorption region [28]. The photodetector with a length of  $24 \mu\text{m}$  offers a good compromise between long wavelength responsivity and having a short length (reduced RC). For comparison, the measured  $-3\text{-dB}$  bandwidth at  $-1 \text{ V}$  of the  $24\text{-}\mu\text{m}$ -long photodetector is 21.6 GHz compared to 13.7 GHz for the  $99\text{-}\mu\text{m}$ -long photodetector.

Other than noise limitations from the transimpedance amplifier itself, the sensitivity of a receiver also depends on the dark current of the photodetector. The absolute dark current scales proportionately with the length of the waveguide photodetector. Hence, another advantage of using a suitably short photodetector is the dark current reduction. Fig. 10 shows the dark current of the  $24\text{-}\mu\text{m}$ -long photodetector at different reverse bias voltages. At a reverse bias voltage of  $-1 \text{ V}$ , the dark current is only 64 nA. It would appear redundant to operate at higher bias voltages, but we have to note that the bandwidth and headroom of the photodetector are also dependent on its bias voltage [20].

Fig. 11(a) shows the frequency response of the  $24\text{-}\mu\text{m}$ -long photodetector at different reverse bias voltages, while Fig. 11(b) summarizes the  $-3\text{-dB}$  bandwidth values of the  $24\text{-}$  and  $99\text{-}\mu\text{m}$ -long photodetectors. At reverse bias voltages below  $-2 \text{ V}$ , the bandwidth degrades rapidly as the bias voltage is reduced. This can be attributed to the insufficient depletion of the “intrinsic” Ge region in the p-i-n junction at low reverse bias voltages. The reduced depletion width essentially increases depletion capacitance. Although the intrinsic region was designed to be undoped, dopants can be introduced into this region as a result of background doping in the epitaxial reactor and dopant diffusion from the highly doped contact regions. At zero bias, the bandwidth of the  $24\text{-}\mu\text{m}$ -long photodetector is only 11.1 GHz. The built-in electric field still enables a limited depletion of the intrinsic region and allows photodetection. However, at such low electric fields, carrier transit time will begin to dominate. As such, the bandwidth improvement of the  $24\text{-}\mu\text{m}$ -long photodetector over

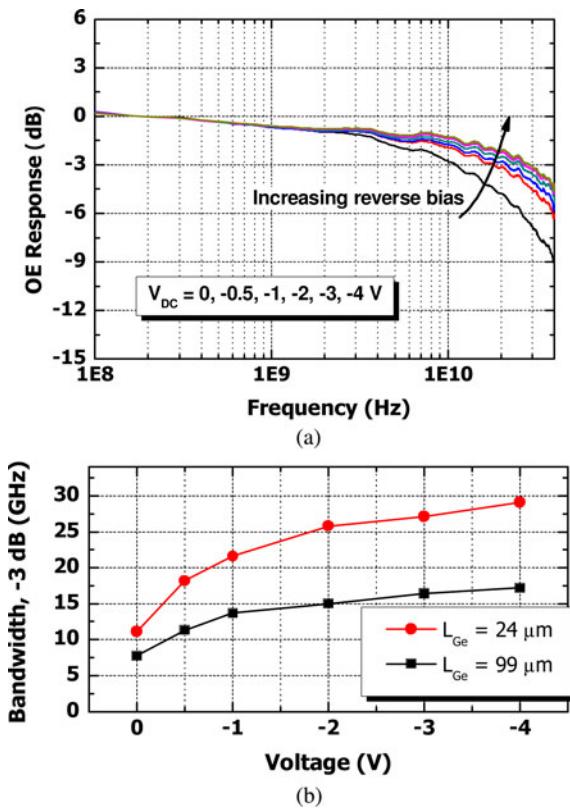


Fig. 11. (a) OE frequency response of a 24- $\mu\text{m}$ -long photodetector. (b)  $-3\text{-dB}$  bandwidth of 24- and 99- $\mu\text{m}$ -long photodetectors at different bias voltages.

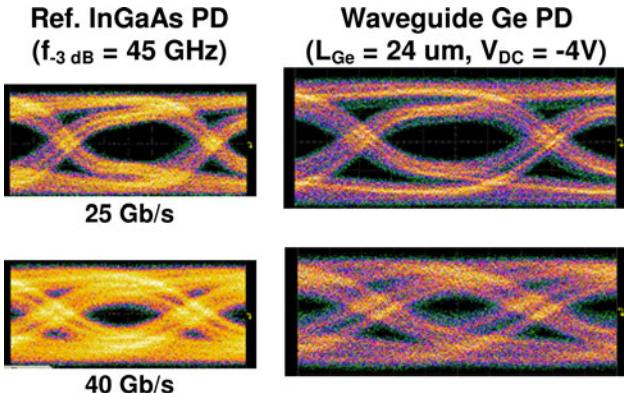


Fig. 12. Eye patterns of waveguide Ge PD at 25 and 40 Gb/s. The eye patterns of an InGaAs photodiode with a  $-3\text{-dB}$  bandwidth of 45 GHz were measured using the same RF test setup and shown as a reference.

that of the 99- $\mu\text{m}$ -long photodetector becomes reduced at zero bias. For very high speed operation, it is preferred to operate the photodetector in the high bias regime ( $-2$  to  $-4$  V), where the bandwidth is stable with bias voltage variations.

Fig. 12 shows the eye patterns of the 24- $\mu\text{m}$ -long photodetector waveguide photodetector at 25 and 40 Gb/s. The eye patterns of an InGaAs photodiode ( $-3\text{-dB}$  bandwidth = 45 GHz) were also measured using the same RF test setup for reference. Unlike the frequency response measurements, the effect of the cables and connectors cannot be de-embedded. It is obvious that the RF test setup is limiting the eye pattern measurement as the Ge

photodetector and the InGaAs photodetector show very similar eye patterns. Nevertheless, it illustrates that the capability of the Ge photodetector to operate at data rates of up to 40 Gb/s.

### B. Electric-Field-Induced Absorption Improvement and Carrier Multiplication Gain

From the previous section, it is obvious that the approach of reducing the length of the photodetector to improve the bandwidth is limited, since there is a point beyond which the responsivity at long wavelengths will be too compromised. In fact, a reduced responsivity directly degrades receiver sensitivity. Lower receiver sensitivity in turn translates into a need for increased transmitted signal power at the source end, and essentially increases laser and cooling-related power consumption. To address the dilemma between length reduction for bandwidth improvement and adequate length for high responsivity at long wavelengths (L-band), we investigate how the responsivity at long wavelengths can be improved by utilizing the Franz–Keldysh effect in a similar concept as Ge electroabsorption modulators [29]–[31]. We further explore how avalanche carrier multiplication can also be used to provide usable gain even in conventional p-i-n germanium photodetectors, consistent with that reported in [32], but with low dark currents.

To demonstrate these effects, we shall examine photodetectors with a very short germanium region of only 5  $\mu\text{m}$  in length. With such a short length, the responsivity rolls off rapidly beyond 1550 nm. Fig. 13(a) plots the normalized responsivity against voltage for two wavelengths of light (1524.9 and 1611.5 nm). The absolute responsivity at 1524.9 nm is  $\sim 0.7 \text{ A/W}$ , which is  $\sim 80\%$  of that for the longer photodetectors discussed in Section III-A at the same wavelength. At 1524.9 nm, the light is almost fully absorbed despite the short length. At 1611.5 nm, only a small fraction of the light is absorbed due to the short length. At 1524.9 nm, it is observed that the responsivity remains constant up to about  $-4.5$  V. At 1611.5 nm, a linear increase in responsivity is observed as the voltage progresses from 0 to  $-4.5$  V. At  $-4.5$  V, the responsivity has increased by 170% over that at 0 V. This increase in responsivity at 1611.5 nm against voltage is attributed to the Franz–Keldysh effect, which is dependent on the electric field applied across the germanium layer. This implies that the Franz–Keldysh effect can possibly be used to increase the long wavelength responsivity in a very short germanium photodetector to a high level.

From  $-4.5$  to  $-9$  V, the responsivity for 1524.9-nm light starts to increase superlinearly with voltage. This occurs due to the onset of avalanche multiplication which effectively increases the number of electron–hole pairs generated for each absorbed photon. The same trend is observed for 1611.5-nm light, but with a faster rate of increase, which is due to the combined effects of avalanche multiplication and the Franz–Keldysh effect. At a bias voltage of  $-8$  V, the responsivity at 1611.5 nm matches that at 1524.9 nm at low bias voltages, due to the combined effects of avalanche multiplication and the Franz–Keldysh effect. Referring back to Fig. 9, we should note that even the 99- $\mu\text{m}$ -long

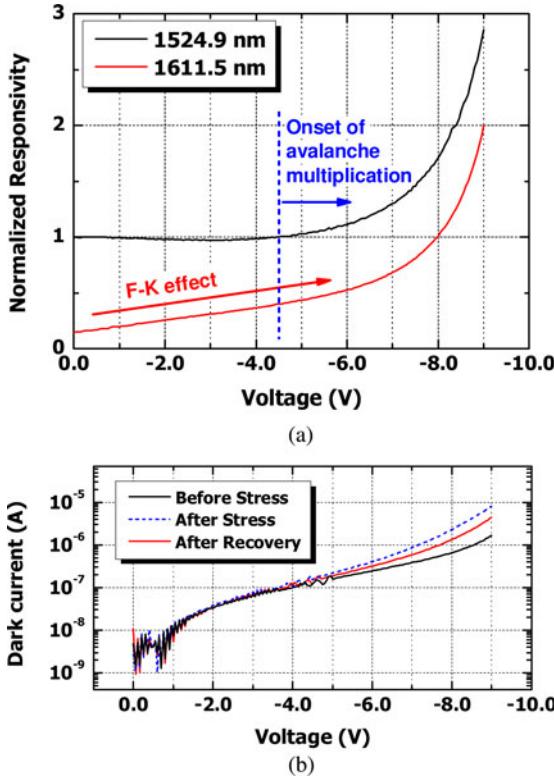


Fig. 13. Plot of (a) normalized responsivity (normalized to responsivity at  $-1\text{-V}$  bias at 1524.9 nm) against voltage for two wavelengths (1524.9 and 1611.5 nm) and (b) dark current against voltage for the 5- $\mu\text{m}$ -long Ge photodetector before electrical stress, after electrical stress, and after recovery.

photodetector could not achieve a normalized responsivity of 1 because of parasitic optical losses in the long absorption region.

The natural question which comes to mind would be the dark current at these relatively high voltages. The black curve in Fig. 13(b) shows the dark current–voltage characteristics of a fresh device (before any high-voltage stress). Because of the small junction area associated with such a small photodetector, the absolute dark current is actually low even at relatively high bias voltages. At a bias voltage of  $-8\text{ V}$ , the dark current is only  $\sim 660\text{ nA}$ . Yet, at this same bias voltage, the photodetector already achieves a gain of 1.7 times at a wavelength of 1524.9 nm, and a normalized responsivity of 1 at 1611.5 nm. This is an absolute responsivity of  $\sim 1.2$  and  $\sim 0.7\text{ A/W}$  at 1524.9 and 1611.5 nm, respectively, which exceed those of the 99- $\mu\text{m}$ -long device at low bias voltages.

To further reap the benefits of avalanche multiplication gain, the applied voltage was increased to  $-9\text{ V}$ . At  $-9\text{ V}$ , the gain is 2.86 times or 4.56 dB. However, we have to note that there are side effects associated with operation at such a high bias voltage. The device was stressed at  $-9\text{ V}$  for 15 min, during which the dark current increased rapidly during the first few minutes after which it stabilized. The dark current–voltage curve, which is plotted in blue dashes in Fig. 13(b), shows an increase in dark current which is increasingly pronounced at higher voltages. This phenomenon may be due to the generation of mid bandgap states which could be located at the germanium to cladding oxide interface. These interface states increasingly contribute to the

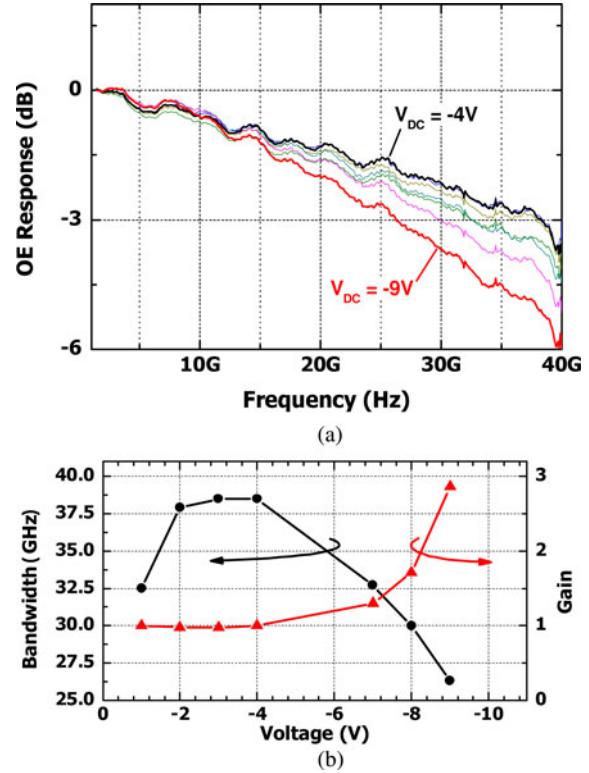


Fig. 14. (a) OE frequency response and (b)  $-3\text{ dB}$  bandwidth and multiplication gain of a 5- $\mu\text{m}$ -long Ge photodetector at different reverse bias voltages ( $\lambda = 1524.9\text{ nm}$ ).

junction leakage as the electric field increases via a trap-assisted tunneling mechanism. It is also interesting to note that the device recovers after several current–voltage sweeps, as shown by the red curve in Fig. 13(b). The phenomenon needs further investigation and can possibly be solved by a better surface passivation approach or even a guard ring.

Another observed side effect is the degradation in bandwidth after the onset of avalanche multiplication gain, as shown in Fig. 14(a) and (b). The device reaches maximum bandwidth (full depletion of the intrinsic layer) at about  $-2\text{ V}$ . At high bias voltages where there is multiplication gain, the bandwidth degrades. At  $-9\text{ V}$ , the bandwidth is only 26.3 GHz compared to 38.5 GHz at  $-4\text{ V}$ . A gain-bandwidth product of 75 GHz is obtained and is limited by the relatively low gain that can be obtained at reasonable dark currents and voltages, and also by bandwidth degradation. The gain-bandwidth product is relatively low compared to those reported of avalanche photodetectors with separate-absorption-charge-multiplication structures [33]–[35]. Due to the small device size, its bandwidth is transit-time limited. A possible explanation for the bandwidth degradation is the additional transit-time-related delay as a result of charge multiplication. First, it should be noted that the “intrinsic” Ge film is actually lightly p-type as grown due to background doping in the epitaxy reactor ( $P^+P^-N^+$  structure). As such, the electric field is highest near the n-type top contact. Let us examine a particular scenario where a photon is absorbed in the depletion region near the p-type bottom contact, generating an electron–hole pair there. The hole would be rapidly collected at the bottom

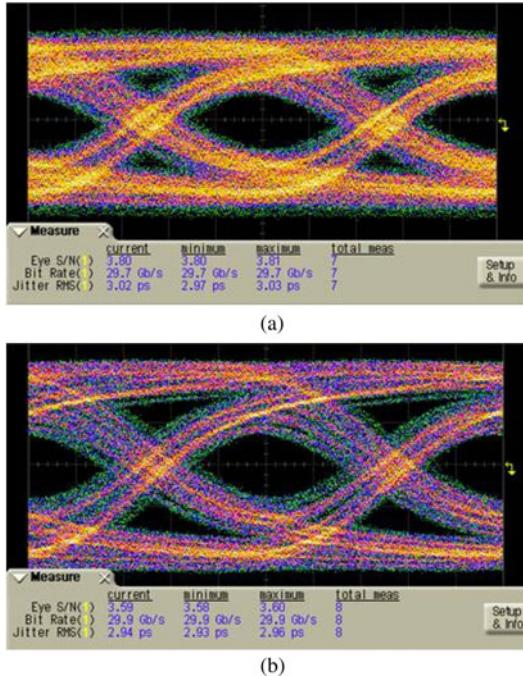


Fig. 15. Eye pattern of a 5- $\mu\text{m}$ -long Ge photodetector at a bias voltage of (a) -4 V (unity gain) and (b) -9 V (4.5-dB avalanche gain).

contact, while the electron drifts to the n-type top contact to be collected. It creates additional electron–hole pairs by impact ionization, starting the avalanche multiplication process. The holes then have to drift to the bottom contact to be collected. As a result, the transit times of the electron and the hole would add up. To improve the bandwidth at high multiplication gain, the aggregate transit time can be reduced by reducing the intrinsic layer thickness in the p-i-n structure.

Fig. 15 shows the comparison between the 30-Gb/s eye patterns measured at -4 and -9 V. The eye pattern at 40 Gb/s is not shown because although the eye is open at 40 Gb/s, it is not clear enough for quantitative signal-to-noise ratio measurements. The signal-to-noise ratio measurements show only a slight degradation for the eye at -9 V to  $\sim$ 3.6 compared to  $\sim$ 3.8 at -4 V. The measured RMS jitter is also comparable at close to 3 ps for both.

Reducing the intrinsic layer thickness would also have the advantage of increasing the electric field in the junction, potentially enabling operation of these avalanche photodetectors at low bias voltages not unlike conventional photodetectors. Low-voltage avalanche operation was reported in metal–semiconductor–metal photodetectors in [36], but lower dark current is desirable. The dark current is likely to increase as a result and would require efforts in surface passivation and germanium film defect reduction to address. The reduction in intrinsic layer thickness also increases the capacitance which will result in RC-limited bandwidth tradeoffs. Overall, this means that a significant amount of process modifications and device parameter optimizations are required, but the end result could have very significant impact on future silicon photonics receivers.

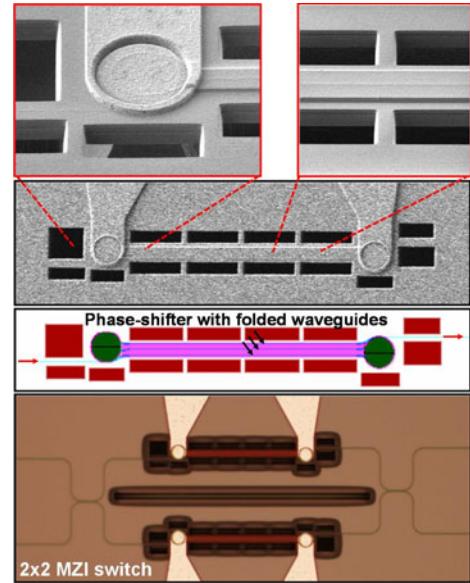


Fig. 16. Optical microscope and SEM images showing a  $2 \times 2$  MZI switch with thermally isolated thermooptic phase shifter arms.

#### IV. HIGH-EFFICIENCY INTEGRATED THERMOOPTICS

Besides carrier-based electrooptics, integrated thermooptics provides an alternative way of actively tuning the effective index of a waveguide and is the focus of this section. The thermooptic tuning mechanism is inherently much slower than the electrooptic carrier-based tuning mechanism. The speed, however, is sufficient for applications in switching, phase-tuning, or simply for integrated heaters enabling temperature control. Thermooptic tuning avoids some disadvantages of carrier-based electrooptics. These are optical losses due to free carrier absorption and the need for forming electrical contacts to the waveguide being tuned. Of course, they can also be used for dielectric waveguides comprising SiN or SiON materials.

For both electrooptic and thermooptic tunings, it is prudent to operate within a reasonable tuning range per unit length of the waveguide. For electrooptic tuning, injecting too high a concentration of free carriers results in heat being generated and is counterproductive since an increase in temperature causes a refractive index change that is opposite in polarity to that caused by increased free carrier dispersion, thereby reducing efficiency. For thermooptic tuning in a semiconductor waveguide (e.g., Si), heating the waveguide to too high a temperature will result in free carrier absorption losses as a result of thermally generated free carriers in silicon.

In view of this, it is beneficial for the length of the phase shifter waveguide to be sufficient to achieve the required tuning range, so as to avoid secondary effects aforementioned. To reduce the footprint while simultaneously improving power efficiency, the waveguides can actually be folded. Fig. 16 shows the optical microscope, design layout, and scanning electron microscope (SEM) images of a  $2 \times 2$  MZI switch using thermooptic phase shifters. The waveguides are folded twice under the integrated heater to allow a single heater to essentially heat up three lengths of the waveguide. To further improve the power

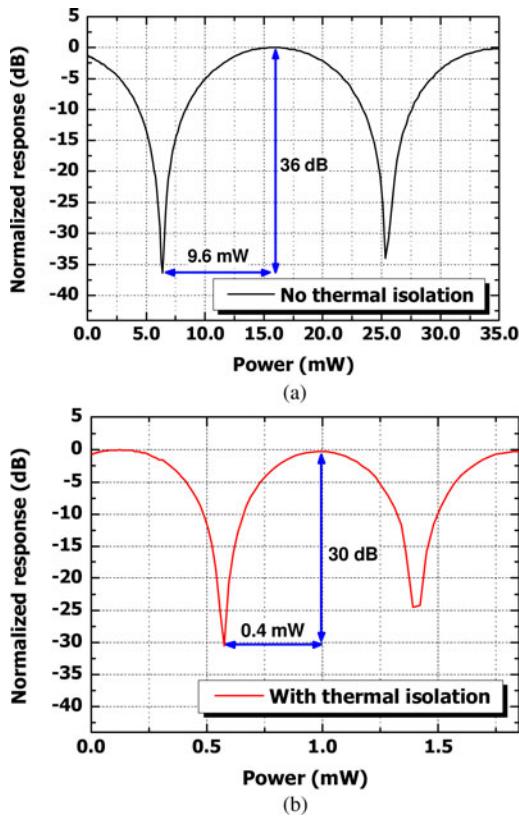


Fig. 17. Normalized output response of one output port of a  $2 \times 2$  MZI switch (a) without thermal isolation and (b) with thermal isolation.

efficiency, thermal isolation was created by using an isotropic plasma etch process to remove the silicon in the substrate layer beneath and around the phase shifter regions. The same process can also be used to fabricate low-loss mode-size converters on the same wafer [37]. Fig. 17(a) and (b) shows the output response for the  $2 \times 2$  MZI switch without and with thermal isolation, respectively. With thermal isolation, a switching power of 0.4 mW was achieved, which is only about 4% of the switching power (9.6 mW) of a similar switch without thermal isolation. Besides improving power efficiency, the on-chip fabricated thermal isolation will also reduce thermal crosstalk between heat-generating devices. It is possible that the extinction ratio for the thermally isolated switch was slightly degraded by the isolation trenches being placed too close to the waveguides, resulting in minute scattering losses and a small amount of power imbalance in the two phase shifter arms. Nevertheless, both switches achieve 30 dB or more in extinction ratio.

A disadvantage with thermal isolation is that the switching speed degrades. Similar observations have also been reported for thermooptic switches in which the thermal isolation was increased by increasing the thickness of the SOI buried oxide thickness [38]. In the thermally isolated switches, the sum of the rise and fall times increase to 645 from 22.8  $\mu$ s, as shown in Fig. 18(a) and (b). As such, there is a tradeoff between speed and power efficiency, which depends on the application. The degree of thermal isolation can be adjusted by layout design changes (varying the width of the phase shifter region between the iso-

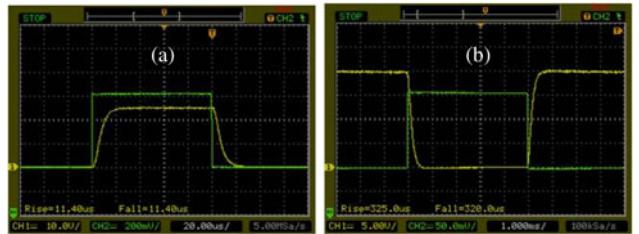


Fig. 18. Temporal response of a  $2 \times 2$  MZI switch (a) without thermal isolation and (b) with thermal isolation.

lation trenches to vary the width of the silicon wall connecting to the underlying silicon substrate).

## V. CONCLUSION

We have discussed three active silicon photonics device technologies which form the core of silicon PIC platform. High-speed operation at 40 Gb/s for both modulators and photodetectors has been demonstrated, and the approaches for scaling toward even higher speed have been discussed. To realize 40-Gb/s modulation at lower drive voltages, the proposed approach is to improve the phase efficiency using more efficient junction designs so that the phase shifter can be shortened, thereby reducing RF loss in the electrodes. Any optical loss penalty incurred can be partially offset with doping compensation. In addition, methods for efficiency improvement have been investigated, including the utilization of high-efficiency doping designs in silicon modulators as well as avalanche multiplication gain and the Franz-Keldysh effect in germanium photodetectors. As the complement to electrooptic index tuning, high-efficiency on-chip thermooptic index tuning was also demonstrated by employing isotropic trench-based thermal isolation. In the not-so-distant future, the silicon photonics PIC platform is expected to revolutionize I/O systems at different distance regimes.

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