Review of Silicon Photonics Foundry Efforts

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(Invited Paper)

***Abstract*—Silicon photonics have progressed to a point where the next step for commercialization depends on the accessibility of manufacturing foundries. The implementation of a fabless foundry model using standardized process technology platforms is crucial for that to occur. Research and development (R&D) foundries are beginning to play bigger roles in transforming silicon photonics into a mature technology for mass production. R&D foundry services such as multi-project wafer (MPW) shuttles, customized process developmental runs and small volume manufacturing are discussed. The development of commercial foundries for low cost, high volume production is also shown to be underway, and key results from an on-going effort to set-up a manufacturing silicon photonics foundry line are presented.**

***Index Terms*—Foundry, manufacturing, multi-project wafer (MPW), photonic integration, silicon photonics.**

I. Introduction

SILICON Photonics has become one of the leading technological solutions for integrated photonics that target applications such as high performance computing, optical communications (telecom/datacom), optical sensors, and on-chip optical interconnects. Over the last two decades, the vision of achieving an optoelectronic integrated circuit has spurred interest in silicon (Si) photonics research [1]. Since then, silicon photonics technology has reached new heights in terms of device performance and levels of integration. This has garnered vast interest in the field due to its tremendous market potential. Recent acquisitions of silicon photonics companies indicate an inflexion point for commercialization in the coming few years [2]–[4].

Complementary metal–oxide–semiconductor (CMOS) technology platform dominated the microelectronics industry in the last 40 over years through the enablement of complex low power electronic circuits with high yields. These foundry lines typically run high production volume wafers with standard process flows where fab loading is generally in the thousands or tens of thousands of wafers per month depending on the CMOS technology node. This is in contrast with the low anticipated volumes for silicon photonics products [5]. The discrepancy in wafer volumes suggests that further scrutiny must be made on how capital-intensive CMOS foundry infrastructure can be reused economically.

Integrated device manufacturers (IDM) that have their own fabrication facilities could be used to set-up specific foundry lines for silicon photonics. However, these are not pure-play foundries, and their accessibility for utilization may be limited due to strategic interests from the respective companies. At this critical juncture, unless concerted efforts are made in developing foundry lines for prototyping and chip fabrication in a high yield manufacturing environment, the vision of low-cost silicon photonics may take considerably longer to realize.

In this paper, we review relevant efforts to develop silicon photonics foundry lines to advance the field. Section II will briefly discuss the adoption of silicon photonics as a fabless semiconductor model, the integration of photonics in standard CMOS technology nodes, and current technology platform. In Section III, silicon photonics foundry services available to the general public for research and development (R&D), and prototyping are presented. These cover both multi-project wafer (MPW) shuttles, and customized developmental runs. Finally, in Section IV, the set-up of commercial foundry lines are discussed together with the importance of a value chain to push silicon photonics towards large scale productization.

II. Silicon Photonics: Current Status

A. Fabless Semiconductor Model

Silicon photonics enables high-level integration of photonic devices onto a silicon wafer. Potentially, this will reduce chip form factor, lower component and assembly costs, and increase chip functionality. It has been established that key photonic components can be monolithically integrated on the same substrate. This has led to the demonstration of high speed silicon photonics platforms in recent years [6], [7]. Device bandwidth of 25 Gbps and beyond will enable a practical low-cost solution for high speed optical communications; currently the most targeted application space in silicon photonics.

Almost all silicon photonics research conducted in academia, research institutes, or industry requires a cleanroom facility to fabricate photonic devices or circuits for testing and design verification. The setting-up and maintenance of an in-house fabrication facility requires millions of dollars depending on the

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real estate, and sophistication of the cleanroom equipment. Not every institution or company owns a facility for silicon wafer processing, and in the absence of such, wafer fabrication has to be outsourced. Research collaborations between academia groups and companies allow fabrication cost to be either subsidize, or entirely waived off. However, these collaborations may not always be feasible because of intellectual property (IP) concerns, especially for private companies.

Therefore, an alternative would be to outsource the chip fabrication as a paid service job to retain the designer's IP. This requires easily accessible foundries with a framework to run silicon photonics processes. Still, it can be costly when full processed wafers are procured, or when customized processes need to be developed.

The field of silicon photonics can progress rapidly if a fabless semiconductor model for silicon electronics (which is largely CMOS) is adopted [8]. Designers would be able to use standard cell designs with known performance specifications for accurate prediction of photonic circuit or system functionality. For this to occur, there must pre-requisites such as:

1) a stable and repeatable silicon photonic process flow;

2) design rules and device library pertaining to the process flow;

3) computer-aided design (CAD) tools for device and circuit simulation;

4) a design platform that incorporates simulation and layout tools.

As with electronics, a method to leverage all of the above is vital to establishing a fabless foundry model. One possible way would be to utilize electronic CAD tools in a CMOS environment, and assimilate the photonic process into a standard CMOS flow [9]. However, it is unlikely that this is sufficient. In the long term, silicon photonics software simulation tools have to be meshed together with CMOS layout tools to offer a more complete design platform.

Once a fabless silicon photonics model is in place, multi-project wafers (MPW) shuttle runs can be organized to reduce overheads associated with chip fabrication through the sharing of photomask and wafer processing costs. In the electronics industry, this is well illustrated by MOSIS, an organization that provides MPW services from various commercial semiconductor foundries for electronics circuit design and innovation [10]. By setting up foundry lines to facilitate a fabless model, this will naturally reduce barriers relating to cost and accessibility for silicon photonics manufacturing.

B. CMOS Photonics Approach

The monolithic integration of silicon photonic devices and CMOS electronics was proposed mainly to create highly densed circuits with reduced parasitics, and achieve lower costs for integration. In this discussion, monolithic integration is defined as photonic and electronic devices formed in the frontend-of-line (FEOL) steps in the standard CMOS flow. There have been early efforts from the electronic-photonic integrated circuit program to develop a platform for electronic and photonics circuit functionality using BAE Systems 0.18 μm CMOS foundry [11]. Photonics devices were demonstrated using the CMOS line, but integration of photonics devices with Si CMOS electronics was not explicitly mentioned.

In 2006, Luxtera made the first breakthrough by announcing its silicon CMOS photonics technology using Freescale's 130-nm CMOS silicon-on-insulator (SOI) technology node [12], [13]. Process modifications to the base CMOS process was made by changing the starting substrate and inserting photonic-related process steps. This enabled a 4×10 Gbps silicon photonics transceiver chip to be built with photonics devices monolithically integrated alongside CMOS electronic circuitry. This technology was used to manufacture active optical cables (AOC) products, and currently remains a closed platform with limited public accessibility. There are on-going efforts to allow more access to the platform which will be discussed in Section IV.

There have been demonstrations of photonic device integration in a CMOS transistor flow without process alterations. This was motivated by efforts to use the CMOS process and foundry infrastructure for photonic device fabrication without change. Orcutt *et al.* used a 28 nm bulk CMOS [14], and subsequently a 45 nm SOI CMOS [15] foundry process, to integrate photonic devices such as poly-silicon (and crystalline Si) waveguides, Si ring wavelength demultiplexing (WDM) filters and modulators with CMOS electronics. It is noteworthy that an electro-optic transmitter was demonstrated using *pin* Si ring resonators and integrated electronics in Ref. [15]. In both CMOS technology processes, post processing was conducted to eliminate losses associated with the optical-coupling to Si substrate due to a lack of a thick buried oxide (BOX) layer beneath the optical devices. This was done by locally removing the underlying Si using XeF_2 etching. Still, these efforts were not able to achieve a reasonably efficient photodetector for light detection. In another recent work, IBM's 0.18 μm CMOS SOI process technology was used to implement waveguides and Si photodiodes without post processing [16]. However, waveguides losses were high and the photodiodes were limited to 850 nm wavelength operation. Overall, the absence of low-loss crystalline Si waveguides, specific optical implants for the active devices, and a suitable light detection material for telecommunication wavelengths makes it extremely challenging to build large-scale high speed photonic systems in a standard CMOS flow without process alterations.

After Luxtera's success, IBM further demonstrated photonics-electronics integration in a sub-100 nm CMOS SOI technology node. Assefa *et al.* monolithically integrated optical modulators and Ge photodetectors into IBM's base 90 nm high performance logic technology node [17]. Primarily, the employment of an advanced CMOS technology node enables the higher speeds from electronic circuitry to match the photonics integrated circuit (PIC) bandwidth. For the 90 nm CMOS integrated Nano-photonics platform, the transistor gate length was additionally scaled down to increase the electronic circuitry bandwidth for a stable 25 Gbps optical receiver performance.

Monolithic integration offers advantages for silicon photonics, but it also introduces complexity in process integration and in the co-designing of photonics and electronic circuitry. The starting substrate itself presents a fundamental difference in which CMOS SOI is optimized for transistor performance and

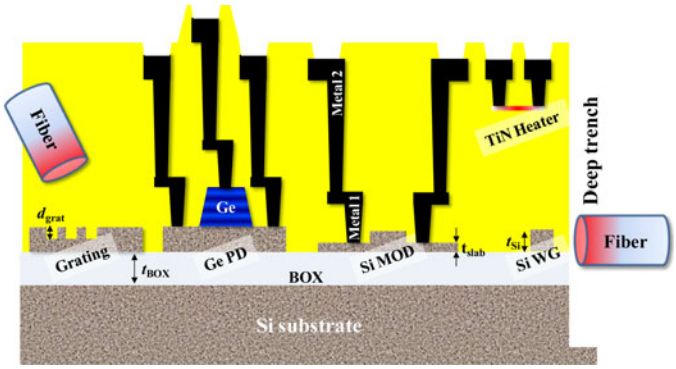

Fig. 1. Cross-section schematic of an integrated silicon photonics platform where key building blocks such as Si passives, Si MOD, Ge PD, thermal optics, and fiber coupling access are shown (Dimensions not to scale). Grating depth (d_{grat}) and slab thickness (t_{slab}) are formed through different partial Si etches.

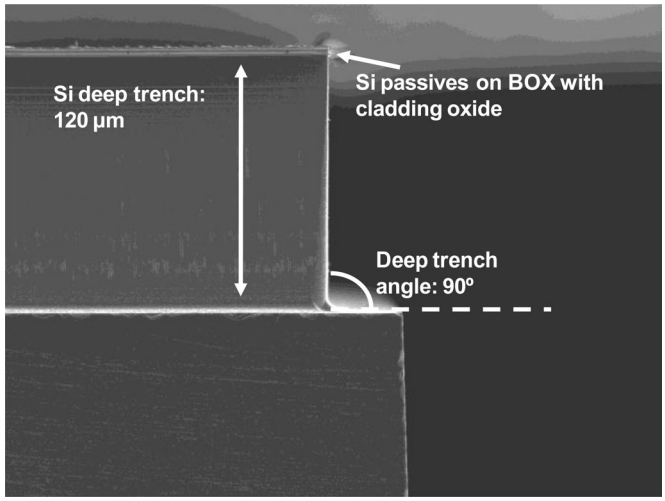

Fig. 2. Cross-SEM image of 120 μm Si deep trench to allow edge coupling access.

low thermal impedance [15], while the photonics SOI uses a much thicker BOX. As the critical dimensions (CDs) scales down for advanced CMOS nodes, there is also a mismatch in device dimensions between the transistors (sub-100 nm) and the photonic devices (0.1–1 μm). Hence, the photonics devices do not make efficient use of "expensive" wafer area in an advanced electronics node. In addition, optimizing the CDs for two groups of devices with an order of magnitude difference in CDs on the same lithographic layer is challenging.

Although integrating photonics onto the same chip as electronics might be advantageous for certain applications, the majority of silicon photonics research is currently concentrated on "photonics only" chips. These are done using the CMOS-compatible tool set in silicon foundries, but without the complication of integrating two different process flows. In the near future, a more compelling approach for photonics and electronics integration is likely to be hybrid whereby the photonic and electronic chips are separately fabricated and connected by wire bonding, bump bonding (flip-chip), or even 3-D die stacking for the longer term [18]. This allows the high speed PIC to be integrated with electronics separately from advanced CMOS or BiCMOS [19] technology nodes. These are relatively easier methods as compared to monolithic integration and provide better cost-performance tradeoffs. For bandwidths of larger than 25 Gb/s, bump-bonding is generally preferred over wire-bonding to reduce parasitics [20].

C. Silicon Photonics Technology Platform

The fabless silicon photonics model described in Section II-A needs a standard process platform consisting of critical photonic device components to be successfully implemented. Yet, versatility in the process platform is also required to support functionality in different applications (for e.g. optical sensing may need an oxide open etch to expose the Si passives for sensing, while high speed datacom may need fiber pigtailing to an edge-coupled PIC). In a way, the development and optimization of silicon photonics process technology is still progressing, and process flexibility has to be exercised. Nevertheless, a convergence towards a generic silicon photonics platform consisting of both passives and active devices is evolving in recent years.

Fig. 1 shows an example of this evolution towards an integrated technology platform. The material-of-choice for the starting substrate in silicon photonics is a SOI wafer. The BOX thickness (t_{BOX}) is typically $\sim$1–3 μm for efficient optical mode confinement in the Si passives. To enable single-mode optical waveguides for telecommunications wavelengths, the SOI top Si thickness (t_{Si}) is usually at least 200 nm. The Si passives are formed by the initial first few mask layers through partial and full Si etching steps. After which, multiple optical implantations are conducted for active devices such as the germanium photodetectors (Ge PD), and Si modulators (Si MOD). Ge epitaxy step is carried out after the Si implants and activation anneal, due to restrictions in thermal budget from Ge (unless a rapid melt growth technique is chosen to incorporate the Ge in a monolithic CMOS frontend [17]). Although Fig. 1 depicts a vertical *pin* Ge PD and Si *pn* Mach-Zehnder (MZ) MOD present in the platform, both the Ge PD and Si MOD can be fabricated in other configurations (for e.g. a lateral *pin* Ge PD, or a Si *pn* ring MOD). Other photonic devices such as WDM filters, and optical switches not illustrated in Fig. 1, can also be formed with a combination of the aforementioned process steps.

In the back-end-of-line (BEOL) metallization steps, a TiN heater can be included for thermal tuning or modulation. The TiN heater allows large area thermal heating (over the Si passives) which is an advantage over doped crystalline-Si heaters that are formed on the same lithographic layer as the Si passives.

The coupling of the optical signal is enabled by edge couplers and Si gratings. For lateral coupling, a Si deep trench is etched to allow fiber access to the edge of the chip. Fig. 2 shows a cross-SEM image of a 120 μm Si trench form by a deep reactive-ion-etching (RIE) process. The Si trench has to be $\sim$90° to allow the fiber to be as close as possible to the PIC for effective coupling. An oxide etch is conducted (before the Si deep trench RIE) to create a smooth oxide facet to minimize light scattering off the sidewall. This facilitates low-loss coupling from the single-mode fiber to the on-chip edge coupler, and eliminates the need for sidewall polishing of the chip after dicing. For die-level

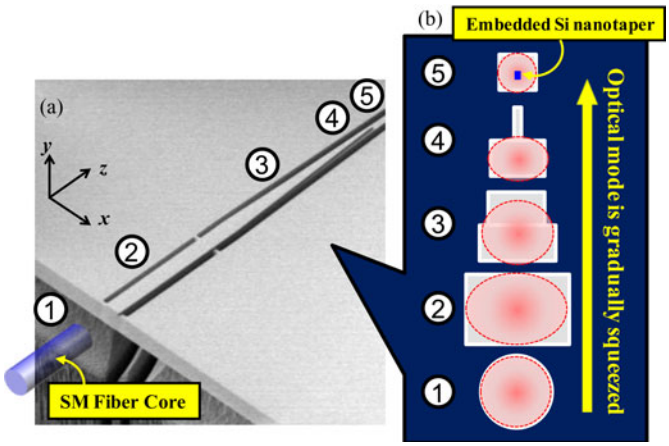

Fig. 3. (a) Tilt SEM image of a suspended oxide mode convertor with a SM fiber shown to illustrate edge coupling. (b) Cross-section schematic to show the optical mode is gradually squeezed as it transits from the SM fiber into the oxide coupler, and eventually the embedded Si nanotaper.

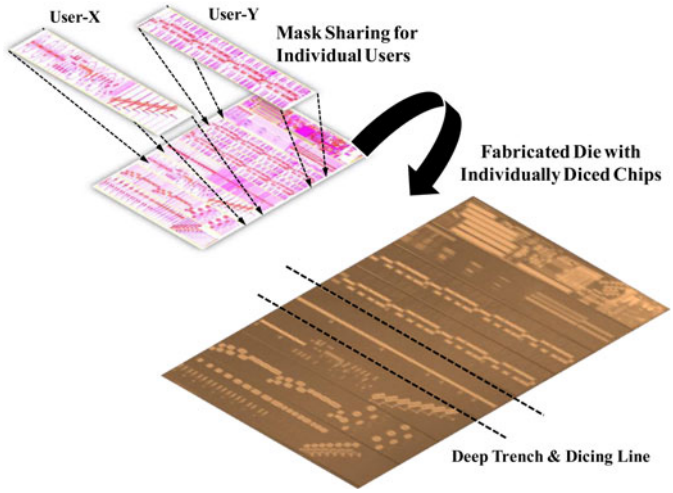

Fig. 4. MPW service allows users to share mask space and fabrication costs by using a fixed process flow.

testing, a ∼180 nm inverted Si nanotaper can be fabricated through the standard Si etches, and used to couple light from a lensed fiber onto the PIC. A coupling loss of ∼2 to 3 dB is achievable from this testing set-up.

For low-loss coupling from a single-mode cleaved fiber, a suspended oxide mode size convertor can be utilized [21]. Fig. 3 (a) shows a tilt SEM image of the suspended oxide coupler. This works as a broadband coupler with an operation range of $>$ 100 nm at 1550 nm wavelength regime. Optical mode profile transition from the SM fiber to the oxide coupler and finally the embedded Si nanotaper is illustrated in Fig. 3(b). The input oxide coupler facet dimension in the y-axis is determined by the total oxide thickness (which includes the BOX thickness). This can be increased to match the optical mode size of the input cleaved fiber. With proper design optimization and the usage of refractive index matching oil, the coupling losses and alignment tolerance can be ∼1–2 dB/facet and larger than 2 μm, respectively. High precision and reliable fiber-to-coupler attachment is enabled through this structure.

Surface coupling can be enabled by a diffractive Si grating (for e.g. 1-D or 2-D). The Si grating takes up a small footprint on-chip and is useful for incorporating wafer-level optical testing functionality. Low coupling losses can be attained from gratings with the appropriate Si thickness and design [13]. Unlike the edge couplers, gratings are narrow-band devices and operate at specific operation wavelength range and polarization.

While the platform in Fig. 1 aims to give a comprehensive coverage of the key building blocks in a fully integrated platform, there will be variations in process technologies developed by different research groups with the omission or inclusion of certain devices.

III. R&D Foundry Service

Over the last 5 years, the speed of silicon photonics research has accelerated, and accessibility to fabrication foundries becomes important to facilitate R&D. R&D foundries are owned either by research institutes that are non-profit organizations and largely funded by the government, or by private companies for internal R&D. Section III looks at R&D foundries from research institutes and the fabrication services offered to the silicon photonics community.

A. Standardized MPW Platform

Various organizations have offered MPW service runs ranging from "passives only" to full integration flows using standardized platforms. Fig. 4 illustrates how multiple users can share a standardized process by owning a portion of the reticle space on a mask set. This can range from small areas of a few square millimeters to large blocks that are tens or hundreds of square millimeters. Wafers are fabricated using a standard process flow, and diced after fab out. From there, individual dies can be chosen and sent to the respective users. This service works because it is unlikely that the entire 200 mm SOI wafer with ∼25,000 mm^2 of usable chip area will be fully utilized for all R&D runs. As such, the total reticle area ranging from 400 to 800 mm^2 per run (depending on the reticle field size) can yield numerous dies for different users. The sharing of mask and a standard process reduces the barrier of entry for silicon photonics research by providing a low cost fabrication path for many academic research groups and fabless companies.

Silicon photonics MPW shuttle runs first started out with "Si passives only" process flows. These had a few masking steps for the Si etches and a fast turnaround time. As silicon photonics research progressed, there was an increasing demand for higher levels of device integration, in particularly the actives. In addition, the fabrication of discrete active devices does not fully exploit the benefits of silicon photonics.

In 2011, optoelectronics systems integration in silicon (OpSIS), co-funded by Intel, was launched to create a silicon photonics foundry service [22]. Based at University of Delaware in the United States, OpSIS coordinates regular shuttle runs for silicon photonics through foundry partners. The goal was to provide inexpensive silicon photonics devices to the community at large that will ultimately allow rapid and reliable system designs. The first MPW service ran at BAE Systems CMOS foundry demonstrated how shared shuttles could be organized

through OpSIS. The following year, OpSIS teamed up with the Institute of Microelectronics (IME) to offer a high speed integrated silicon photonics platform of passive and active devices on 200 mm SOI. This collaboration combines IME's state-of-the-art fabrication facilities and existing silicon photonics process flow, with OpSIS's design and testing capabilities. Since then, multiple shuttle runs have been scheduled in a year to provide quick turnaround times for interested users. Active devices like Si *pn* ring modulators, travelling wave Si *pn* MZ modulators, and vertical *pin* Ge photodetectors have been developed to support a 30 GHz photonics platform [6]. The platform is further evolving to achieve a full device library that allows wavelength interoperability between 1310 and 1550 nm.

In Europe, ePIXfab have similarly been offering silicon photonics foundry service through core partners IMEC and CEA-LETI [23]. These had originally come in the form of Si passives and individual active devices (either IMEC's Si MZ modulator, or CEA-LETI's Ge photodetector) MPW service. Recently in 2013, ePIXfab announced the launch of fully integrated silicon photonics platforms from both institutes. The platforms are also on 200 mm SOI and carry a suite of passive and high speed active devices for PIC design. Data rates of 25 Gbps are achievable from these platforms and this is the bandwidth benchmarked to Luxtera and IBM's 90 nm platforms. The push for full developmental platforms by OpSIS and ePIXfab represents strong interest from silicon photonics fab users in terms of fabrication needs.

To augment the fabrication services, design tools were concurrently developed with software companies by both OpSIS and ePIXfab. A design platform that includes optical device and circuit simulation, layout editing and design rule check (DRC) is required to replicate the success that CMOS electronics experienced through the use of electronic CAD tools. These tools will form part of the process design kit (PDK) associated with the relevant foundries. Mentor Graphics Pyxis has beenone of the selected design platforms by OpSIS and IMEC, while there are a number of software packages such as Lumerical, IPKISS, and Phoenix for photonic simulation needs to choose from.

There are also collaborations with packaging partners to offer fiber-to-chip attachment for ease of chip testing and to build up silicon photonics packaging technological solutions. To complement these MPW services, workshops and seminars are also organized to educate users on the MPW platforms in areas pertaining to fabrication process, design tools and the state-of-the-art technology in silicon photonics. The pricing between the three MPW services is also compared. This represents a significantly reduced cost, as compared to a one-on-one fabrication service job. The basic reticle cost for a 20 plus mask-level process (typical of a fully integrated Si photonics flow) without including wafer processing costs is in the region of a few tens of thousands of dollars. Table I gives a comparison of the silicon photonics MPW services offered by these R&D foundries.

TABLE I
COMPARISON OF FULLY INTEGRATED SILICON PHOTONICS MPW PLATFORM (WITH PASSIVES AND ACTIVES) AVAILABLE IN R&D FOUNDRIES

	IME/OpSIS	IMEC/ePIXfab	CEA-LETI/ ePIXfab
Passives	Si passives with 60nm, 130 nm and 220 nm etch depths	Si passives with 70nm, 130 nm and 220 nm etch depths, extra poly-Si layer	Si passives with 70nm, 130 nm and 220 nm etch depths
Photodetector	Ge vertical *pin*	Ge vertical *pin*	Ge lateral *pin*
Modulator	Si MZ, Si ring	Si MZ, Si ring	Si MZ
Heater[1]	doped Si	doped Si	---
Couplers	Vertical and edge	Vertical	Vertical
Wavelength Supported[2]	1310 and 1550 nm	1310 and 1550 nm	1550 nm
CAD Tools	Mentor Graphics/ Lumerical	Mentor Graphics/ IPKISS/Phoenix	Mentor Graphics/ Phoenix
Packaging	PLC Connections/ Chiral	Tyndall National Institute	Tyndall National Institute
Pricing[3]	\$1800 - 2200 USD/mm^2	\$1330 – 1550 EUR/mm^2	\$1400 – 2500 EUR/mm^2

Note: MPW platforms are based on a 200 mm SOI (220 nm Si/2 μm BOX) substrate. All information is extracted from Ref. [22] and [23].
[1]TiN heater is offered in CEA-LETI/ePIXfab standard passives flow but not indicated in full platform
[2]1310 nm support is mentioned for both IME/OpSIS and IMEC/ePIXfab's platforms
[3]Pricing depends on block size, number of users and discounts offered.

B. Customized Process Platform

The standardized MPW platform provides a route for low cost fabrication, and is beneficial to foundry users to do initial silicon photonics designing. As R&D developmental efforts progress, sometimes design innovation alone is unable to achieve the desired PIC performance. New foundry users may also request for custom-made processes that the standard MPW platform cannot support. Therefore, process customization of the technology platform is required to meet end-user specifications, and it is important that the R&D foundries can offer this flexibility because customized developmental runs with a commercial semiconductor foundry would require a significant amount of investment.

For example, IME is a R&D foundry that offers customized prototyping to its foundry users. For the fully-integrated platform supported by IME (shown in Fig. 1), it can either be offered as it is, or modified to cater to different process technological requirements. This can come in the form of process enhancements to the platform such as integrating a dual Si-SiN waveguide system [24], or adding an oxide release step to form suspended thermal phase-shifters [25]. These enhancements increase functionality of the platform and improve device parameters which may be absent in a standard MPW flow. Sometimes, novel devices which entail a slightly more deviated process from the standard platform are also investigated for different application needs [26], [27]. Generally, process customization should only be done if performance tradeoffs largely outweigh the additional process complexity involved.

C. Small Volume Production

Right now, Luxtera and Kotura are the only notable companies processing wafers for silicon photonics products. Luxtera used Freescale's 200 mm foundry as a manufacturing line for its AOC product, while Kotura has an in-house 150 mm foundry line used for both R&D and manufacturing of its variable optical attenuator (VOA) products [28].

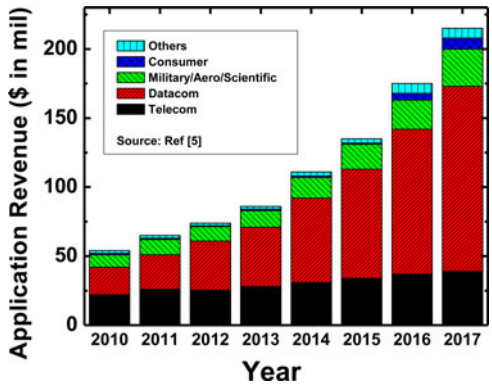

Fig. 5. Silicon photonics application revenue from 2010 to 2017. The total revenue is forecasted to be slightly over $200 million dollars in 2017 with the largest portion coming from datacom.

The volume for silicon photonics products is not anticipated to be large in the next couple of years mainly because of the low initial volumes for new technology products, and the lack of a high volume killer application in the mass market. Fig. 5 shows the application revenue for silicon photonics products from 2010 to 2017 [5]. The expected silicon photonics application revenue in 2017 is slightly above $200 million dollars with the largest revenue coming from datacom applications. This current estimation translates to very small percentage of the total optical communications market size of ∼$ 9.5 billion dollars.

As such, preliminary volume for silicon photonics applications is predicted to be a few hundreds of wafers per year, and this is a mismatch in business model for CMOS foundries engaged in high volume manufacturing [29]. At this stage, there is a need to find foundries to handle small volume manufacturing so that the gap between prototyping and high volume production can be filled. R&D foundries could therefore, bridge this gap. However, these foundries need to be set-up to cope with the increased wafer volumes, while keeping processes stable to meet product specifications. These include stringent statistical process control (SPC) monitoring and inline metrology checks, strategies to meet tight schedules in product lot cycle times, and a transition path for high volume manufacturing when the wafer volume ramps up in the future.

IV. Commercial Manufacturing Foundry

Although Section III describes the foundry services and models available to develop silicon photonics R&D, companies are still hesitant to invest in product development unless there is a clear design for manufacturability (DFM) path. This includes 1) the manufacturing foundry of choice, once the proof-of-concept is validated, and 2) the technology transfer mechanism that would occur between R&D and manufacturing phases. Till date, there is no open access commercial foundry available for mass production of silicon photonics chips. As more companies look towards developing silicon photonics products, there are increasing demands for dedicated silicon photonics foundry lines to enable low cost manufacturing.

From the supply side, CMOS foundries invest a huge amount of capital (for e.g. billions of dollars for advanced CMOS nodes) into equipment and cleanroom facilities. Full utilization of these facilities to maximize profitability is a must for silicon CMOS foundries. The time and cost spent on developing new process technology in the foundry without foreseeable return-of-equity (ROE) will drastically reduce profit margins, and is typically not undertaken.

Naturally, silicon photonics companies are reluctant (or sometimes unable) to commit wafer volumes directly to the commercial foundries without a product feasibility study. This involves prototyping at a foundry line, and an evaluation before mass production. However, this has invariably led to a "chicken and egg" situation whereby there are no compelling factors for CMOS foundries to undertake huge developmental efforts in building up a silicon photonics manufacturing line without ROE commitments. Yet, without a foundry line,silicon photonics companies find it difficult to advance the technology for commercialization. Furthermore, the struggle to find high volume opportunities for silicon photonics reduces the attractiveness of this technology to CMOS foundries.

Despite this, silicon photonics technology has reached a point whereby elements in a supply chain, particularly a manufacturing facility, have become critical for technological development and commercialization. As such, Section IV presents on-going efforts in setting-up silicon photonics foundry lines for mass production.

A. Luxtera-ST Microelectronics Collaboration

In 2012, Luxtera and ST Microelectronics (STM) announced a collaboration to develop a silicon photonics line at STM's 300 mm facility in Crolles, France [30]. The technology will be a "photonics only" integrated platform which is different from the monolithic electronics-photonics integration scheme adopted for Luxtera's AOC product. As mentioned in Section II-B, this allows hybrid integration of the PIC with advanced electronic node of choice. For photonics-electronic integration, the suggested approach would be face-to-face bonding i.e. flip-chip for this platform.

The technology transfer leverages on Luxtera's Freescale 130 nm CMOS SOI process using a 300 nm Si / 800 nm BOX SOI starting substrate. The device library is expected to have extended wavelength interoperability for 1310 nm and 1550 nm; other than 1490 nm, the wavelength used for Luxtera's AOC. An open-source Cadence-based Si photonics design environment is also being refined for PIC design support. This collaboration effort is expected to provide low cost, high volume manufacturing for silicon photonics components and systems. It also marks the first time that Luxtera's silicon photonics platform will become accessible to the public.

B. Leveraging CMOS Foundry Infrastructure

In a similar effort, IME, GlobalFoundries (GF), and Bell Labs, Alcatel-Lucent (ALU) have collaborated to develop a silicon photonics process technology platform for the industry. This technology development was done on GF's 200 mm 0.18 μm CMOS manufacturing foundry line with ALU providing design support. GF's 0.18 μm CMOS foundry line was selected to

provide low cost processing in a stable manufacturing environment with high yield. To get an estimate of the cost difference between CMOS technology nodes, the cost per mm^2 in a MPW shuttle for a 0.18 μm CMOS node (Logic, Mixed mode/RF) was compared with a 90 nm CMOS node and found to be $\sim$5 times cheaper [31]. It is anticipated that silicon photonics chip cost per mm^2 in a manufacturing foundry can be cheaper than the R&D foundries shown in Table I, especially when a less advanced CMOS technology node is utilized. Using 0.18 μm CMOS prices in Ref [31] as a lower limit, a reduction in cost per mm^2 (from prices in Table I) by a factor of half is possible. However, cheaper prices are not guaranteed and depend largely on the business strategies adopted by the manufacturing foundries, since low wafer volumes are almost certain in the initial stages of commercialization.

A 220 nm Si/ 3 μm BOX SOI platform was used to develop photonic devices as shown in Fig. 1. FEOL process steps such as Si etch and optical implants were standard manufacturing processes in GF's 0.18 μm fab. GF's BEOL process was used for a two-level metallization consisting of tungsten (W) plugs and Aluminium (Al) metal. The inter-layer dielectric and inter-metal dielectric used is purely oxide. This facilitates surface coupling by minimizing dispersion due to dielectric material refractive index differences and interface effects. A silicon nitride (SiN) layer was employed for passivation and can be removed at areas where surface coupling is required. Process modules are individually verified (in terms of functionality) during the technology transfer to ensure that specifications can be met in the final fully integrated platform. Interim results for two important modules (the Si passives and waveguided Ge *pin* PD) in this transfer are presented.

Wafer-level testing is essential for the manufacturability of silicon photonics. It serves as a means for inline monitoring, process uniformity control, and yield improvement for silicon foundry processing. This ensures that only known good dies (KGD) are selected for packaging or further integration with electronics or the laser diode after fab out.

CMOS foundries have electrical test blocks placed at the wafer scribe lines to serve as process control monitoring (PCM) structures. Wafer-scale electrical testing can likewise be employed for silicon photonics on these PCM structures to monitor the electrical characteristics of active devices, in particular, the Ge photodiodes and Si modulators. For active devices, wafer-level electrical measurements which are standard to CMOS are important to determine device performance, uniformity and yield. This can be done with commercial electrical probe stations in the foundries.

Having electrical testing is not sufficient for photonics device characterization. A wafer-level optical testing platform has to be developed together with the process technology platform for a silicon photonics manufacturing foundry line. This ensures that product wafers meet specifications before chips are delivered to the customer. Currently, wafer-scale optical testers are not as commercially available as electrical testers. It will take time before silicon photonics testing methodology can evolve to be as streamlined as Si CMOS. Presently, wafer-scale optical testers are built through customization by various organizations for photonic device testing [6], [13].

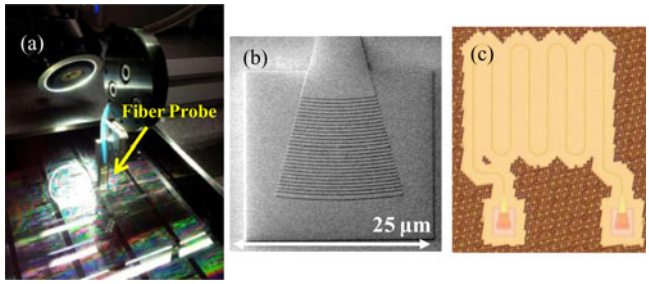

Fig. 6. (a) Wafer-level optical tester set-up with a fiber array used for I/O optical ports. (b) SEM image of a Si grating used for wafer-scale measurements. (c) Optical micrograph of grating coupler with Si channel WG used in cutbacks to extract WG propagation loss.

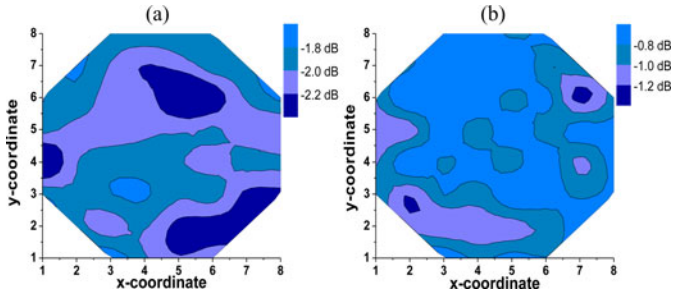

Fig. 7. Wafer-level map of (a) Si channel waveguide and (b) Si rib waveguide losses from a Si passives pilot wafer fabricated in GF. The WG width was 500 nm and slab thickness for the rib WG was 90 nm. Average WG loss was $\sim$2 and $\sim$0.8 dB/cm for Si channel and Si rib WG, respectively. A total of 52 dies were measured.

Fig. 6(a) shows an image of an optical wafer-level tester set-up in IME for automated testing. The tester uses a fiber array (with 127 μm fiber pitch) as the optical probes. During measurements, the fiber probe is $\sim$20 μm above the wafer (in the z-axis). A "golden" Si passive wafer is used as a test set-up reference before measurement to ensure that the fiber probe condition and set-up parameters remain consistent. DC and RF electrical probes can be mounted to the tester for electrical-optical (EO) measurements when needed. Grating couplers are used are the optical I/O ports on the wafer for the optical measurements. Fig. 6(b) shows a SEM image of a typical Si grating. For waveguide (WG) propagation loss extraction, Si WG attached to the gratings are used in cutback structures [Fig. 6(c)].

A pilot Si passive wafer (without SiN passivation layer) was fab out from GF's line and measured. The Si channel and rib WG propagation loss of $\sim$2 and $\sim$0.8 dB/cm were attained, respectively, at central wavelength (see Fig. 7). Tight optical propagation loss distributions with standard deviation of $\sim$0.2 dB/cm were obtained for both WGs from the first run. There was no post-etched treatment or optimization done to the Si waveguide formation process. Bending loss for a 5 μm Si channel WG bend (width of 500 nm) was measured to be 0.016 dB per 90° bend. Measurements at 1550 nm were also extracted for these devices and similar results were attained in terms of losses and distributions.

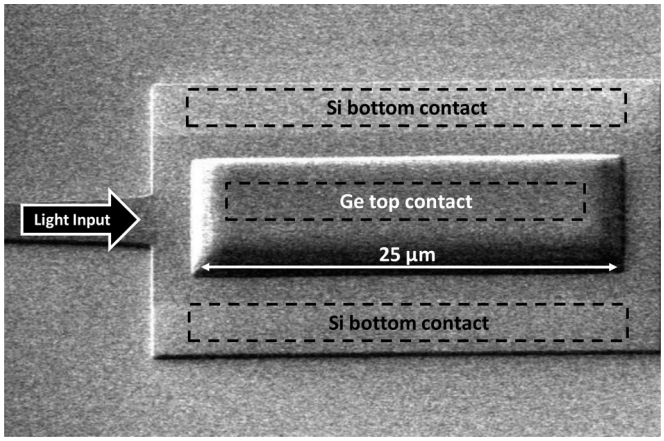

Fig. 8. SEM image of selective epitaxial Ge film grown on Si mesa for waveguidedGepin PD fabrication. The field oxide which acts as a mask during the epitaxy process has been stripped.

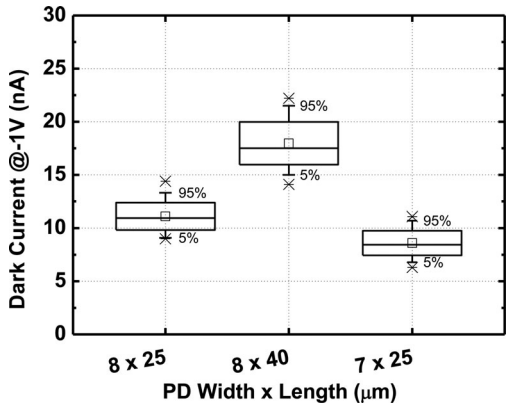

Fig. 9. Tight statistical distribution for waveguided vertical *pin*Ge PD dark current was measured at −1 V reverse bias at different device dimensions. A total of 52 dies were measured from a full 200-mm wafer.

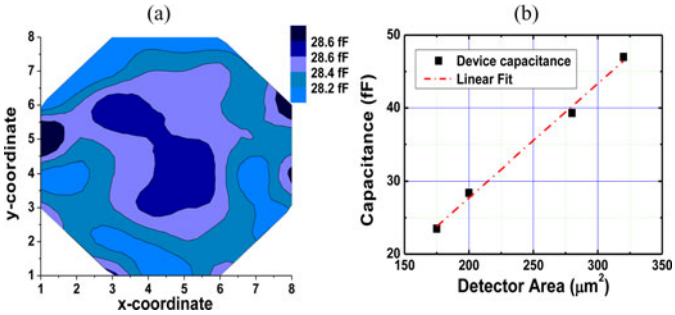

Fig. 10. (a) Device capacitance at −1 V bias plotted in a wafer map showing excellent uniformity with mean capacitance of 28 +/− 0.28 fF for 8 × 25 μm PD. (b) The device capacitance scales linearly with varying detector area.

The mean (and median) central wavelength was at 1538 nm with a standard deviation of 2.8 nm. These gratings were not optimized for best efficiency (with coupling loss of ∼6 dB), and were basically used for wafer-level testing. The coupling efficiency can be improved by 50% using non-uniformed grating couplers [32]. Various low loss passives such as Y-junctions and waveguide crossings can also be fabricated on the current SOI substrate (with a top Si of 220 nm) [33], [34].

Next, pure Ge PDs were fabricated and verified in GF line as well. Although $Si_{1-x}Ge_x$ alloys have been used in advanced CMOS nodes as embedded source/drains in transistors, the largest Ge concentration used is only ∼50% [35]. Therefore, pure Ge is regarded as a "new" material in a mainstream CMOS foundry line. The integration of Ge into the CMOS manufacturing line was done carefully, as a precaution against adversely affecting other production lots running in the foundry line. A specially-tuned epitaxy recipe was used to selectivity grow Ge in exposed Si areas. Waveguided vertical *pin* Ge PDs using this recipe was fabricated on this platform. Fig. 8 shows a SEM image of the Ge grown using the same recipe on an internal IME patterned wafer (as a control wafer for device monitoring purposes).

A Ge PD pilot wafer from GF foundry line was pulled out after Metal 1 for measurements to verify device performance. Statistical plots of the PD dark current for different dimensions are shown in Fig. 9. The uniformity of the dark current is extremely good for a pilot wafer. For a 8 × 25 μm Ge PD, the average dark current was ∼11+/−1.3 nA at −1 V reverse bias. A forward current of more than 10 mA at 1 V was also obtained, giving a forward current to dark current ratio at ± 1 V of $\sim 10^6$. A total of 8 different PDs with dimension and design variations were measured per die with 100% yield (not shown). The dark current density is ∼5–6 mA/cm^2 for all the PDs. This is one of the lowest for an integrated Ge PD [36]–[38], and indicates the low defect density of the Ge epitaxial film.

Device capacitance was also measured for the all PDs with excellent uniformity. Fig. 10(a) shows the wafer map of the 8 × 25 μm PD having a mean capacitance (at −1 V) of 28 +/−0.28 fF. This confirmed that Ge epitaxy process had good thickness uniformity and that all other PD related processes such as implant, dopant anneal, and contact etch were well-controlled. Fig. 10(b) showed that average capacitance varies linearly with the detector area of different dimensions.

Light at 1550 nm wavelength from a tunable laser source (TLS) was coupled into the photodetector through the grating coupler. Due to the lack of a feedback loop for the photodetector (via an output grating coupler), fiber array alignment was done on a standard grating aligner structure before moving to the PD for measurement using a fixed set of x, y coordinates. The aligner structure consisted of an input and output grating with short Si WG (∼90 μm) in between. No additional optical alignment was conducted after the fiber array had moved to the input grating coupler of the detector. The grating ensured that only TE polarized light was input into the PD. Fig. 11 shows the *IV* characteristics of the PD under dark and illuminated conditions. The photocurrent was more than 4 orders higher than the dark current at –1 V. For internal responsivity calculations, the grating coupling loss and Si WG propagation loss was decoupled from the laser power to get the input power into the Ge PD. Average responsivity of 1.06+/-0.15 A/W at -1 V reverse bias was calculated for 16 measured dies. The integrated PD had high responsivity and low dark current characteristics which are crucial to enhance optical receiver sensitivity. The 3dB bandwidth measured was larger than 20 GHz at -1 V at 1550 nm

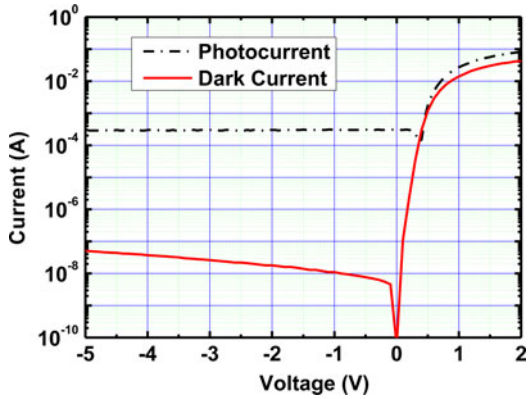

Fig. 11. Dark current and photocurrent (at $\lambda = 1550$ nm) for 8×25 μm waveguided vertical *pin* Ge PD. There are more than four orders of difference between the photocurrent and dark current of the PD at -1 V reverse bias.

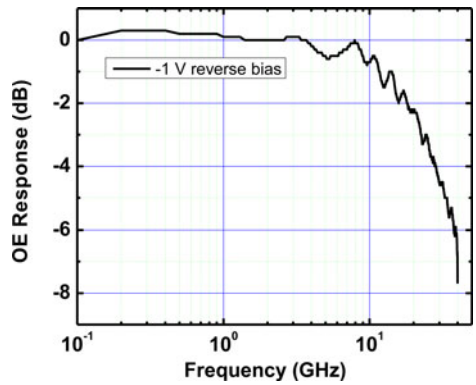

Fig. 12. 3 dB bandwidth of 8×25 μm waveguided vertical *pin* Ge PD showing > 20 GHz at -1 V.

wavelength (see Fig. 12) and is sufficient for 25 Gb/s operation. The current detector design is that of a baseline control PD, and not optimized for higher bandwidth. The PD bandwidth can easily be improved by direct scaling of the detector area to reduce the device capacitance. Detector responsivity is not expected to degrade through scaling given the "thick" Ge (> 500 nm) used for the PD. Metal via offset designs can be additionally used to boost responsivity, if required [37].

Other photonics devices like the Si MOD, and TiN heater have already been integrated with the Si passives and Ge PD in a full flow. The current results gives an indication of expected device functionality after integration, and these will be presented in due course.

C. Process Qualification and Reliability

For a commercial CMOS foundry, both process qualification and long term reliability tests have to be conducted to fully qualify a technology platform for production. These reliability tests follow the American National Standards Institute accredited JEDEC standards for microelectronics qualification.

Thus, a qualification process is also expected for a silicon photonics platform running in a CMOS foundry line to ensure that reliable components and chips are fabricated. For optoelectronic reliability, the Telcordia Standard is usually used to provide

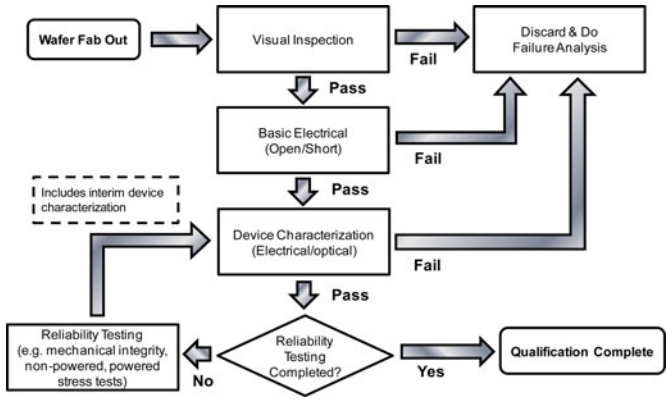

Fig. 13. Reliability test flow for silicon photonics platform qualification at a manufacturing foundry line.

reliability assurance requirements [39]. Optoelectronic products in telecom applications are expected to have operational lives on the order of 20 years. These products are generally made from conventional materials such as silica, III–V and lithium niobate. Going through the qualification tests assesses if these products are able to meet the stringent reliability criteria. Likewise, it is essential that photonics devices made on silicon wafers for similar applications satisfy these criteria too.

Process qualification includes electrical characterization of the PCM structures for e.g. sheet and contact resistances, Ge and Si diode IV, electro migration (EM) test, as well as device characterization. Once the device specifications are met and process optimization is completed, the process is freezed and qualification lots are run for reliability testing. Reliability testing highlighted in Telcordia can be categorized broadly into mechanical integrity tests, non-powered stress tests, and powered stress tests. For silicon photonic chips fabricated in a manufacturing semiconductor foundry, a diode-level (or chip-level) qualification would apply. A flow chart for a general reliability test flow for silicon photonics chip qualification is depicted in Fig. 13. Only KGDs will be used for reliability testing after initial inspection and device characterization is conducted. Since a full qualification timeline stretches to a couple of months, a pre-qualification criteria (e.g., shorten stress cycles, or hours) can be set to allow the initial release of the foundry process for use.

D. Silicon Photonics Value Chain

Fig. 14 illustrates the value chain needed to create a complete silicon photonics ecosystem. The emergence of silicon photonics fabless companies that specialize in PIC designs have generated relevant IPs in the field which may be commercialized into viable photonics products. These fabless companies may be engaged for PIC designing services by photonics product manufacturers (e.g., components, subsystems, systems). Large photonic companies could also perform design in-house and bypass the need to outsource this task. Regardless, silicon foundries described in this study are essential to supply chip fabrication facilities to these companies for PIC prototyping and manufacturing.

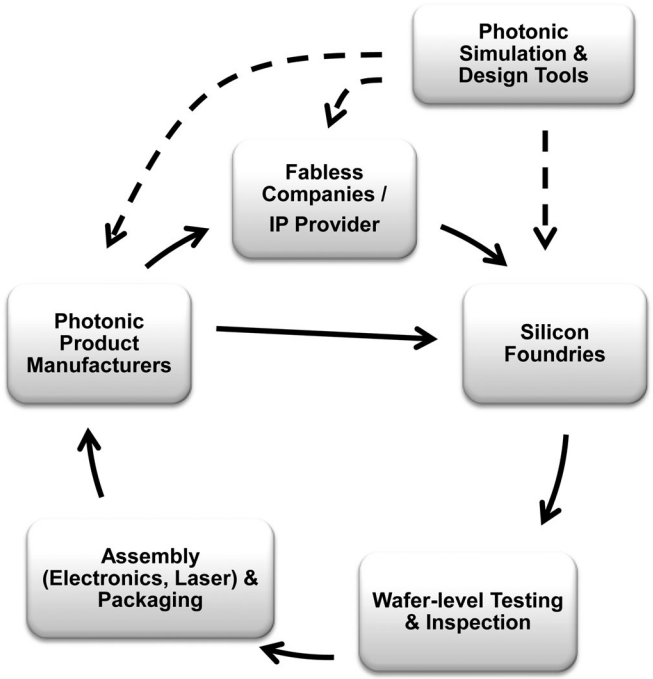

Fig. 14. Silicon photonics value chain consisting of key elements like fabless design companies, CAD tools, silicon fabrication foundries, testing and inspection facilities, assembly and packaging houses, and the photonics product manufacturers.

Software companies that develop design tools for device modeling and circuit simulation support the value chain by creating a design platform for silicon photonics. A well-equipped silicon photonics PDK that offers simulation and layout tools is necessary for the companies and foundries to execute an efficient fabless model described in Section II-A.

After fabrication, there is a need for wafer-level inspection and testing. Semiconductor test equipment vendors will have to develop wafer-scale optical testers for PIC testing to pick out KGDs. This can be done either by foundries internally with these optical testers, or outsourced to companies that provide optoelectronics testing services. Test equipment manufacturers can sometimes provide these testing services too. Once the KGDs are selected, subsequent integration of the PICs with electronics and the light source are done in assembly houses before the final packaging for the photonic product manufacturers. The value chain should as much as possible leverage existing infrastructure from the semiconductor industry in both testing and packaging aspects which aligns with the framework for establishing silicon photonics foundry lines.

V. Conclusion

A fabless model is imperative for silicon photonics to imitate the success of CMOS electronics. As such, there is a need to standardize silicon photonics processes to a generic platform that encompasses a comprehensive suite of passive and actives devices. Monolithic integration of silicon photonics and CMOS electronics may be an option, but there are still cost-performance tradeoffs to consider. Hybrid photonics-electronics integration holds greater advantages for a short- to near- term approach towards commercialization.

R&D foundries have expanded fabrication services to include fully integrated platforms for MPW and prototyping runs as a way to meet increasing demands from the silicon photonics community. Major efforts to develop commercial foundries for low cost manufacturing have already begun and are to be ready in the coming year. Further strengthening of other important elements in the value chain will allow silicon photonics to advance technologically and overcome the barriers for mass production.

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