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Resistive Memory Devices at the Thinnest Limit: Progress and Challenges

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The Si-based integrated circuits industry has been developing for more than half a century, by focusing on the scaling-down of transistor. However, the miniaturization of transistors will soon reach its physical limits, thereby requiring novel material and device technologies. Resistive memory is a promising candidate for in-memory computing and energy-efficient synaptic devices that can satisfy the computational demands of the future applications. However, poor cycle-to-cycle and device-to-device uniformities hinder its mass production. 2D materials, as a new type of semiconductor, is successfully employed in various micro/nanoelectronic devices and have the potential to drive future innovation in resistive memory technology. This review evaluates the potential of using the thinnest advanced materials, that is, monolayer 2D materials, for memristor or memtransistor applications, including resistive switching behavior and atomic mechanism, high-frequency device performances, and in-memory computing/neuromorphic computing applications. The scaling-down advantages of promising monolayer 2D materials including graphene, transition metal dichalcogenides, and hexagonal boron nitride are presented. Finally, the technical challenges of these atomic devices for practical applications are elaborately discussed. The study of monolayer-2D-material-based resistive memory is expected to play a positive role in the exploration of beyond-Si electronic technologies.

1. Introduction

Since the first commercial microprocessor was introduced in 1971, the semiconductor industry has exhibited substantial progress, from integrating 2300 transistors in Intel's 4004[1] to sixteen billion transistors in Apple's M1[2] processor. Over the past 50 years, with the feature size of a transistor being continuously scaled down, significant progress in materials and manufacturing methods (primarily focused on Si semiconductor technologies) has been achieved; however, we are also witnessing that Si technology is about to reach its physical limits, and new materials and devices compatible with Si technology for future in-memory computing technology should be developed.[3] In recent years, the conventional bulk-Si-based semiconductor technology has encountered a bottleneck in meeting emerging data-intensive industry requirements such as machine learning, Internet of Things, and piloted driving.[4–6] With the rapid development of big-data industries, high-performance hardware, including multifunctional sensors, high-frequency electronics, and computing devices for future sensing, communicating, and calculating, are in high demand. Among various contenders, resistive random-access memory (RRAM) devices, including memristor and memtransistor (multiterminal transistor that combine the functions of memristor and transistor) based on different application scenarios, are promising candidates for achieving in-memory technologies in the near future.

In 1971, an electrical component called memristor was designed and proposed by Chua.[7] In 2009, it was first integrated into complementary metal-oxide-semiconductor (CMOS) circuits by Hewlett–Packard, forming an 8 × 8 crossbar array.[8] In this memristor-CMOS hybrid integrated circuits, the function of memristor is to control the signal transmission among the gates of different CMOS. Although this hybrid integrated chip just provides an FPGA-like functionality, successful integration shows that a single memristor device is able to accomplish functions that require several transistors in a traditional CMOS circuit. Thus, a new memristor-CMOS hybrid architecture that is compatible with the standard CMOS process was developed.[8]

Although Moore's law can be extended beyond the transistor scaling limit by achieving an equivalent circuit action with fewer resistive switching (RS) devices, the integration density of the resistive devices must also be improved for achieving complex computing functions. Multiple investigations spanning over a period of a decade or more have accelerated the integration of RRAM devices;[9–13] moreover, until recently, a NeuRRAM chip

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The ORCID identification number(s) for the author(s) of this article can be found under https://doi.org/10.1002/adma.202307951

DOI: 10.1002/adma.202307951

integrating 3 million RRAM cells was proposed.[9] The RRAM cell in this multicore architecture chip is a HfO_x-based memristor, in which the thickness of switching (HfO_x) and thermal-enhancement (TaO_x) layers are ≈50 nm. Currently, RRAM devices are primarily based on metal-oxide materials such as TiO_x, TaO_x, HfO_x, SiO_x, and ZrO_x.[14] Despite the application of metal-oxide memristor-based chips, which exhibit significant prospects in neuromorphic computing and artificial intelligence,[9,13] the process technology and integration level are still lagging far behind the application requirements. As RRAM devices are continuously miniaturized for achieving more complex capabilities,[9,15–18] the defects will become uncontrollable, and the reliability of devices will be reduced as the thickness of these metal-oxide materials is scaled down to 3 nm.[19] Conventional RRAM devices typically have a vertical metal–insulator–metal (MIM) structure with two terminals. When an electric field is applied, atomic rearrangements or diffusions in devices occur around interfaces or defects such as vacancies, grain boundaries (GBs), and atomic dislocations leading to the resistance switching.[20] Because the resistance of a RRAM device is due in large part to the thickness of the switching layer, as the dielectric layer thickness being scaled down to 3 nm, the local nonuniformity and random defects will have a critical impact on the switching invariability.[19,21] Even a tiny fluctuation in these thinner dielectric layers could lead to a substantial variation among devices.[19] As the thickness of switching layer decreasing, the impact of defects will be amplified. Furthermore, the possibility of metal atoms accumulation will be further aggravated, which also threatens the switching reliability.[19,22] Hence, new types of resistive devices based on alternative materials with lower leakage current and larger ON/OFF ratio are required.[15] Compared to traditional metal oxides based RRAM devices, the RRAM devices based on 2D layered materials have a higher precision in adjusting electrical properties[20] and a better characteristic in miniature. Hence, the application of 2D layered materials in resistive memory devices is discussed subsequently.

2. 2D–CMOS Hybrid Microchips for Memristive Applications

The 2D-material-based RRAM, innating the characteristics of layered materials, should be suitable for 3D device integration. Moreover, a weak van der Waals (vdW) interaction in layered materials provides a feasible bond-free integration technology without lattice or fabrication restrictions.[24] Exploring excellent properties of 2D materials is necessary for fabricating 2D-material-based micro/nano electronic circuits.[23,25–28] However, owing to the local defects in 2D materials, the integration density remains low. Recently, a high-integration-density 2D/CMOS hybrid microchip was presented for memristive applications.[23] The chip is fabricated on a 200 mm Si wafer using an industrial 180 nm CMOS technology node, as shown in **Figure 1**a. In this study, 5 × 5 one-transistor-one-memristor (1T1M) crossbar arrays are demonstrated for the chip integration (Figure 1b,c). The industrial fabrication processes for the hybrid microchips are shown in Figure 1d–g. As seen in the cross-sectional scanning transmission electron microscope (STEM) image of the 1T1M cell in Figure 1h, the lateral size of the resulting memristor is below 0.053 μm^2 based on ≈6 nm thick *h*-BN. Notably, the endurance of this multilayer *h*-BN based RRAM device reaches 2.5 million cycles when sequences of pulsed voltage stresses are applied. However, the switching speeds are still not sufficiently fast (t_{SET} is ≈232 µs and t_{RESET} is ≈783 ns). Although the hybrid 2D/CMOS microchip presented in this work is still far from commercial application, it is the best performance and highest technology readiness level ever achieved in high-integration-density electronic devices/circuit based on 2D RRAMs at the current stage.[23] More importantly, this work demonstrates that 2D-materials-based memristive devices can be applied to the current micro-nano electronic technology.

3. The Scale-Down of 2D Materials-Based Resistive Switching Device in Thickness

Next-generation semiconductor technology requires a size reduction in both the length and thickness of the device.[29] Owing to the bond-free advantage of 2D materials in the out-of-plane direction, they can be easily scaled down to sub-nanometer in thicknesses. As the thickness of these vdW materials reaches their thinnest limit, dielectric materials can become as thin as single-layer atomic sheets. Compared with other materials, atomically thin 2D materials could provide a chance of using atomic-scale manufacturing technology to achieve resistive memory with both planar and vertical device configurations. Therefore, the application of monolayer 2D materials can undoubtedly help overcome the existing process limitations. Theoretically, these 2D monolayers have no restrictions in terms of stacking on other materials; for example, they can be assembled together with completely divergent material constructions, characters, or dimensions because lattice matching is no longer required.[24,30,31] The atomically sharp surfaces without dangling bond open opportunities for the future multifunctional 3D integration. More importantly, 2D monolayer materials still exhibit the potential to achieve a nonvolatile memory (NVM) switching characteristic due to the interactions of defects and their migrations.[32] Thus, the exploration to realize resistive memory devices based on 2D monolayer materials will promote the development of advanced computational and storage technologies in the future.

In this review, the latest progresses of using 2D monolayer materials for resistive memory device applications are systematically introduced, including switching properties, atomic mechanisms, high-frequency performance, and in-memory computing devices/synaptic devices. The scaling down advantages of promising monolayer 2D materials that are applied to atomristors (RRAM devices based on monolayer 2D materials with vertical MIM structures) and memtransistors [planar field-effect transistors (FETs) based on 2D monolayers with NVM characteristics] are presented (**Figure 2**a-l). A more detailed discussion is provided subsequently. Practical applications of 2D monolayer materials in RRAM and other electronic technologies require the growth of high-quality atomic sheets on wafer-scale substrates and low levels of metal atom contamination.[39] Furthermore, the analysis of ultrathin 2D atomic configurations and exploration of their unique electronic and chemical properties will aid innovation. Notably, the study of 2D-monolayer-materials-based resistive memory devices is still at an early stage. A systematic summary and review of the current advancements will help in clearly observing the development trends of this technology and provide

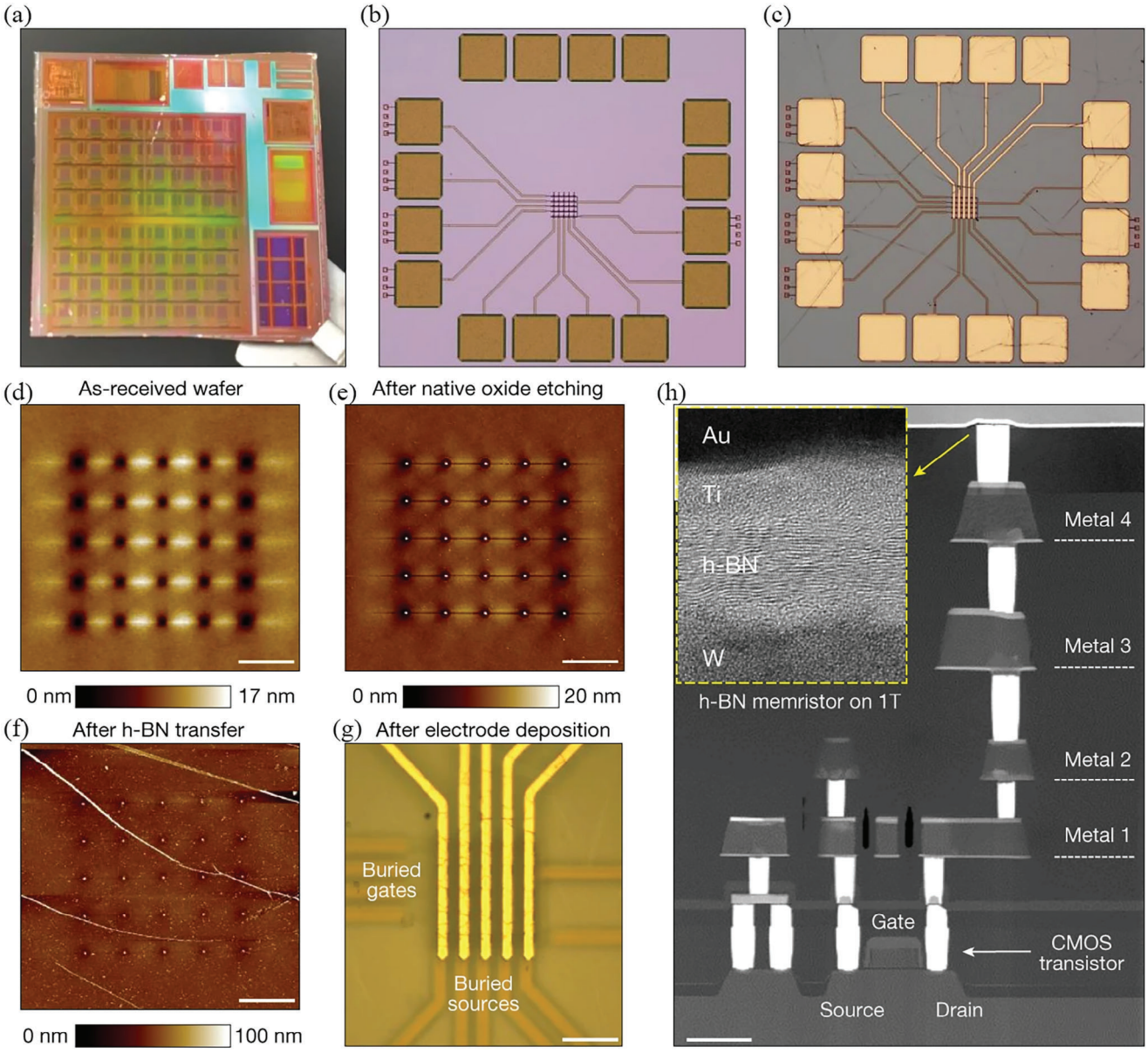

Figure 1. Fabrication of hybrid 2D/CMOS memristive microchips. a) Photograph of the hybrid microchips. Optical microscopic images of a partial microchip containing a 5 × 5 one-transistor-one-memristor (1T1M) crossbar array b) as-received, and c) after fabrication. Topographic maps collected with atomic force microscopy of the vias in the 5 × 5 crossbar arrays on the wafers d) as-received, e) after native oxide etching, and f) after the transfer of the hexagonal boron nitride (*h*-BN) sheet. g) Optical microscopic image of a finished 5 × 5 crossbar array of 1T1M, i.e., after *h*-BN transfer and top electrodes deposition. h) High-angle annular dark-field cross-sectional STEM image of a 1T1M cell in the crossbar array. The inset, which is of 20 nm × 16 nm, shows a cross-sectional transmission electron microscopy image of the Au/Ti/*h*-BN/W memristor on the via; the correct layered structure of *h*-BN can be seen. Reproduced with permission.[23] Copyright 2023, the authers. Published by Nature Publishing group under a Creative Commons Attribution 4.0 International License (CC BY 4.0).

important suggestions for future practical research and development.

4. Application of 2D Monolayer Materials in Atomic Threshold Switching Device

Currently, the volatile threshold switching (TS) characteristic of monolayer 2D materials is primarily observed in single-layer *h*-BN.[40–42] Atomic threshold switches based on monolayer *h*-BN exhibit a low threshold voltage (V_{th}) and high ON-OFF ratio.[41] However, the accumulation of metal atoms due to excessive metal-ion diffusion into the dielectric layer is an important reason for the failure of atomic TS devices with vertical MIM structures.[40] Consequently, the control of active atomic diffusions and formation of uniform filaments are critical for improving the performance of these devices. Atomic-scale defect engineering in graphene can modulate both volatile and nonvolatile resistive switching modes in MIM structures.[34,43] Recently,

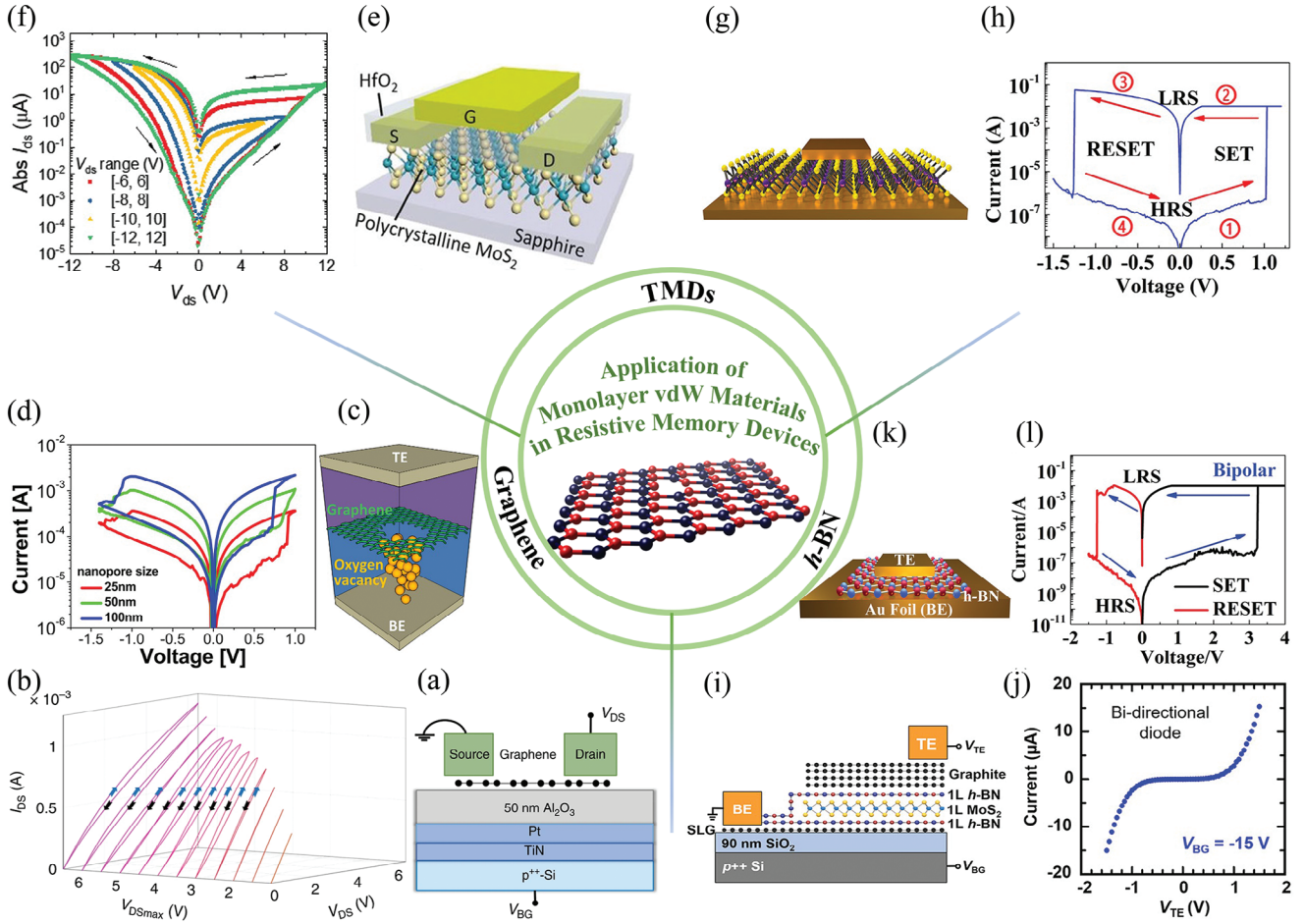

Figure 2. Applications of 2D monolayer materials in resistive memory devices. a) Schematic of a monolayer graphene (MLG) based resistive memtransistor device with planar structure and b) its output characteristics. Reproduced with permission.[33] Copyright 2020,the authers. Published by Nature Publishing group under a Creative Commons Attribution 4.0 International License (CC BY 4.0). c) Schematic of the MLG inserted memristor structure and d) *I*–*V* characteristics of the Ta/MLG/Ta_2O_5 devices with different sizes of nanopores fabricated in the MLG layer. Reproduced with permission.[34] Copyright 2016, American Chemical Society. e) Schematic of a fabricated monolayer MoS_2 memtransistor in a top-gated field-effect-transistor planar configuration and f) I_{ds}–V_{ds} characteristics of the device at diverse V_{ds}. Reproduced with permission.[35] Copyright 2019, John Wiley & Sons. g) Schematic of an atomristor with vertical structures based on transition metal dichalcogenides (TMDs) monolayer and h) its representative *I*–*V* curves. Reproduced with permission.[36] Copyright 2018, American Chemical Society. i) Side-view schematic of the monolayer-*h*-BN/monolayer-MoS_2/monolayer-*h*-BN heterojunction memory selector. Graphite and single-layer graphene (SLG) act as electrodes for estimating the tunneling current. j) Tunneling current change over V_{TE} with $V_{BG} = -15$ V. Reproduced with permission.[37] Copyright 2021, American Chemical Society. k) Schematics of an atomristor based on single-layer *h*-BN and l) its representative *I*–*V* curves. Reproduced with permission.[38] Copyright 2019, John Wiley & Sons.

experiments demonstrate that a defective graphene monolayer can be used to control the formation and rupture of filaments at the atomic level. Thus, the performance of atomic TS devices based on monolayer *h*-BN with volatility can be improved.[40] As seen in **Figure 3**a, without the insertion of a graphene monolayer in a TS device, Ag filaments are randomly formed during the switching process, which results in large variations in the switching characteristics. Conversely, by inserting a graphene monolayer as an ionic barrier in the device, the filament sizes are more uniform (Figure 3b). A graphene monolayer with deliberately created atomic vacancies could effectively modulate the transportation of metallic ions from the electrode, and the performance of the resistive device could be reformed.[40,41] The investigations confirm that the achievement of TS device by inserting a defective graphene monolayer could significantly reduce the variability and improve the reliability by controlling the formation process of conductive filaments, while the threshold voltage is increased (Figure 3c–g) and the switching speed will be reduced (see Figure 3h,i). Hence, balancing the performance parameters for these atomic TS devices is important.

5. Application of 2D Monolayer Materials in Planar Resistive Memory Device

5.1. Application of Monolayer Graphene in Planar Resistive Memory Device

As an application of the typical 2D monolayer material, the concept of graphene-based NVM device has been proposed as early as 2008.[44] As seen in **Figure** 4a, the device is a

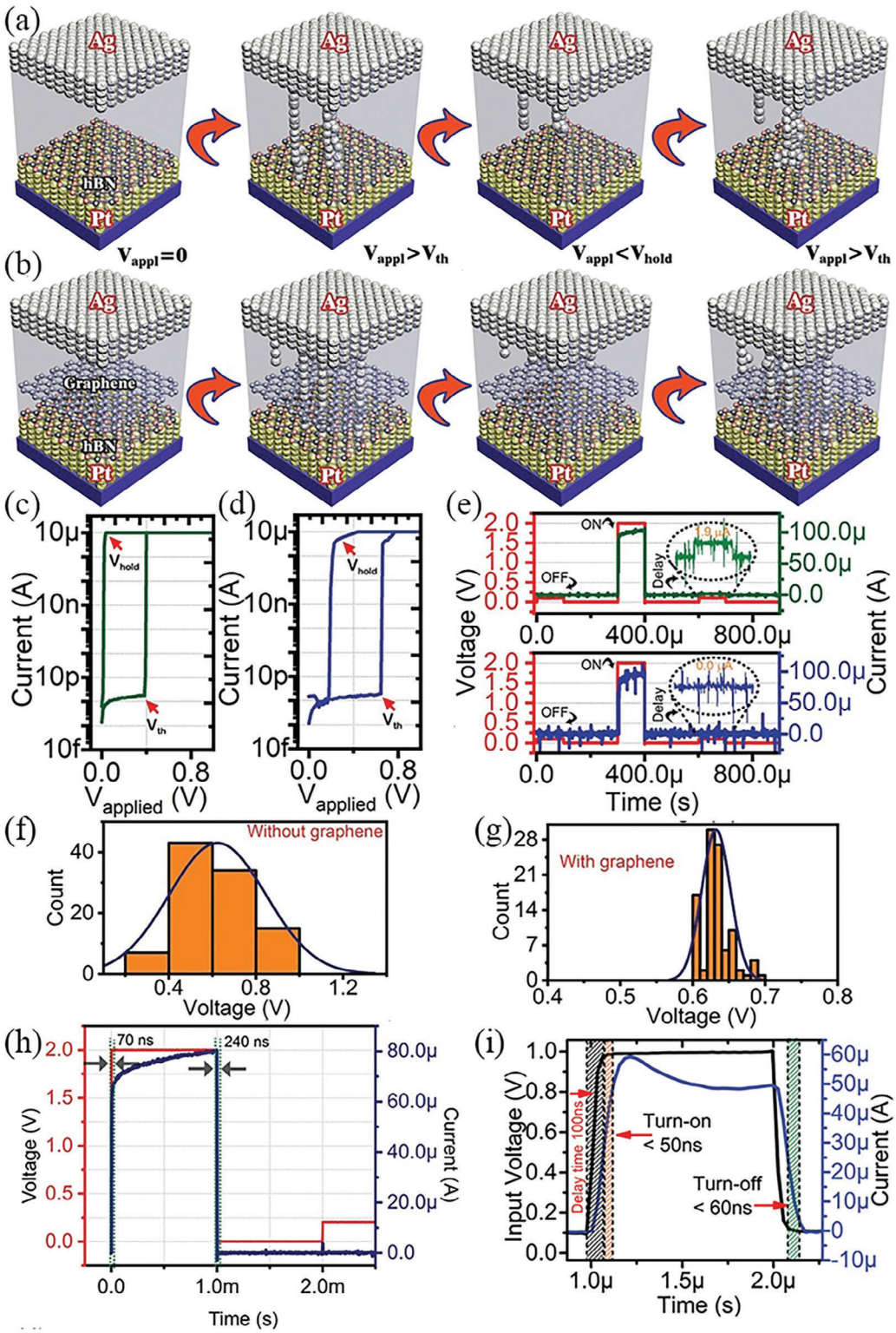

Figure 3. Characteristics of atomic threshold switch based on a single-layer *h*-BN with and without a graphene monolayer acting as an ionic barrier. Conductive filament formation and rupture processes of the atomic threshold switch based on a single-layer *h*-BN a) without and b) with a graphene as a block layer for Ag ions. Resistive switching behavior of the threshold switch c) without and d) with the insertion of graphene. e) Stability of the conductive filaments formed in the *h*-BN threshold switch without and with graphene inserted. Statistical threshold voltage (V_{th}) distribution of the switch f) without and g) with graphene inserted. h) Switching speed of the device with graphene inserted. a–h) Reproduced with permission.[40] Copyright 2022, John Wiley & Sons. i) Switching speed of the device without graphene inserted. Reproduced with permission.[41] Copyright 2021, John Wiley & Sons.

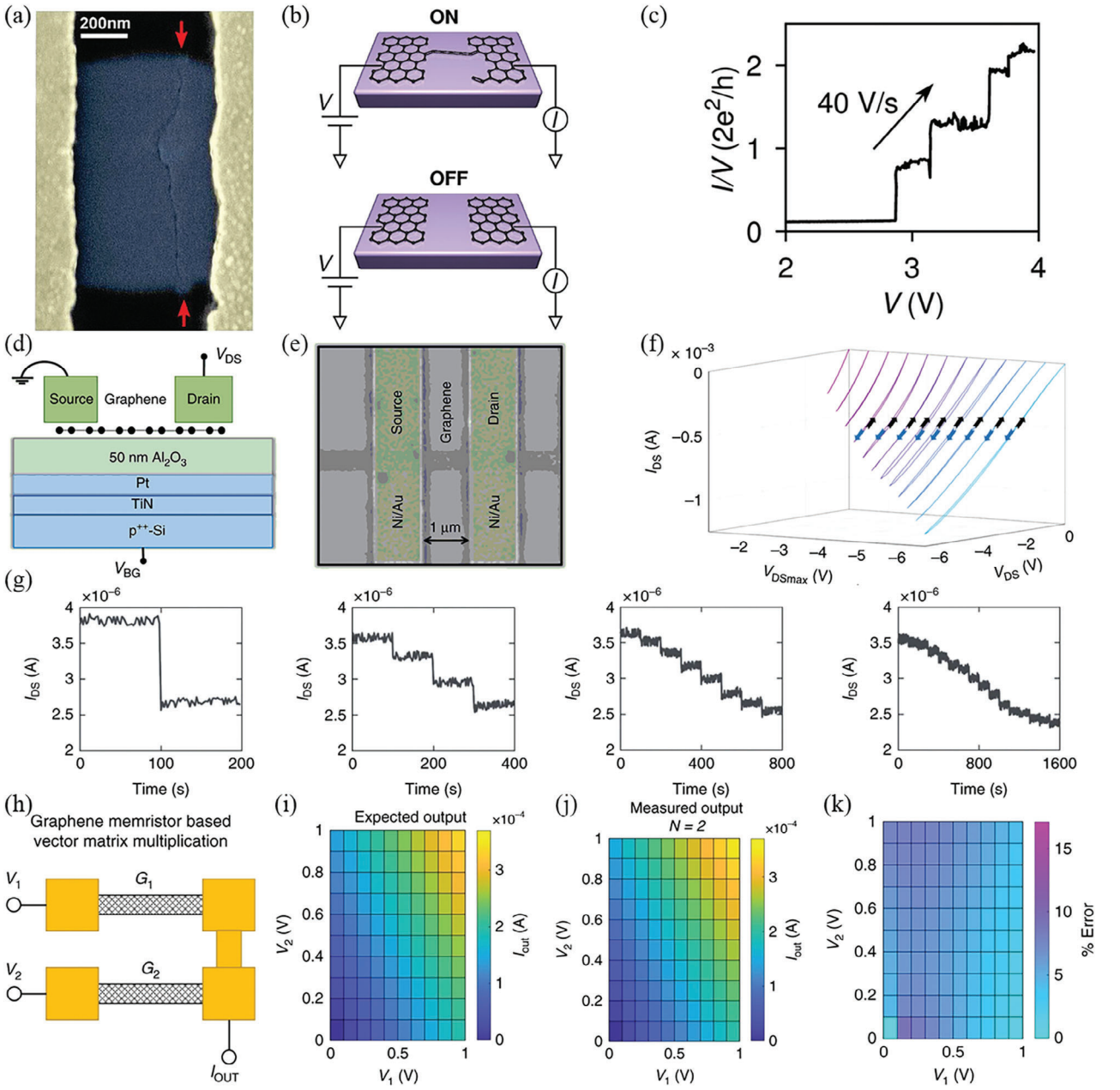

Figure 4. Resistive switching devices with planar structures based on monolayer graphene. Resistive switching device based on monolayer graphene and a) its scanning electron microscope (SEM) image after breakdown. b) Schematic of the device in the ON and OFF states. c) Conductance I/V measured when the device switches from the OFF to ON states. a–c) Reproduced with permission.[44] Copyright 2008, American Chemical Society. d) Schematic of graphene based memtransistor and e) its SEM image. f) Output characteristics of the memtransistor at V_{BG} (back-gate voltage) = 0 V with V_{DSmax} sweep ranging from −1 to −6.5 V. g) Memtransistor exhibiting 2, 4, 8, and 16 conductance levels. h) Vector matrix multiplication based on graphene memory. V_1 and V_2 are drain voltages acting as the input vector, and the conductance values (G_1 and G_2) of the graphene memtransistor acted as the weight matrix. I_{OUT} (output current) is the output vector. i) Colormap of expected I_{OUT} varying with input voltage vectors. j) Experimentally obtained I_{OUT}, and k) error when the weights are rounded to the nearest conductance states following k-means clustering. N denotes the number of analog memory levels. d–k) Reproduced with permission.[33] Copyright 2020, the authers. Published by Nature Publishing group under a Creative Commons Attribution 4.0 International License (CC BY 4.0)

two-terminal device with a planar structure. By controlling the formation and rupture of the C atomic chain (Figure 4b), the device could be switched between the ON and OFF states. Moreover, multiple conductance states are also observed in this two-terminal device (Figure 4c). Although the device works within a vacuum chamber and the switch speed is ≈100 ms, which is significantly slower than the requirement for NVM (≈10 ns),[45,46] this investigation opens the door for the application of monolayer 2D materials in resistive switching devices.

Graphene-based FET resistive devices (referred to as memtransistor here) have also attracted attention over the past 10 years.[44,47] However, achieving multilevel memory on a device unit is still a challenge, which hinders its application in artificial neural networks (ANNs). Recently, a monolayer-graphene-based nonvolatile memtransistor device possessing more than 16 resistance states was reported.[33] As seen in Figure 4d, the device has a planar FET-type structure, and the graphene monolayer acts as the conductive channel (Figure 4e). The output characteristics of the memory are presented in Figure 4f. From the I_{DS}–V_{DS} [i.e., the source-to-drain current (I_{DS}) versus the drain-to-source voltage (V_{DS})] curves, we can observe that the device hysteresis window initially increases with V_{DSmax}. While the V_{DSmax} is beyond −5.5 V, the window of the hysteresis loop starts to decrease. The hysteresis behavior indicates a RS effect. Figure 4g exhibits the values of each conductance state varying with time within 100 s. As the device is programmed into 2, 4, 8, and 16 conductance states, the memory ratio is diminished between adjacent states. The multilevel conductance provides much flexibility for neuromorphic computing applications, allowing for single memory device to achieve targeted weight values as needed. Then, vector matrix multiplication is fabricated (as seen in Figure 4h) based on the monolayer graphene memory array. Figure 4i exhibits the expected I_{OUT} (output current) varying with different input voltage vectors. The experimentally measured I_{OUT} as the memtransistors are rapidly programmed to the nearest conductance states can be seen in Figure 4j. The error for measured I_{OUT} diverging from the expected I_{OUT} is presented in Figure 4k, which is significantly low. Although the resistive switching mechanism behind is still confusing, it is probably related to the dissociation and adsorption processes of H_2O at the graphene/Al_2O_3 interface. This investigation exhibits the benefits of applying a graphene monolayer in resistive switching device, as its memtransistor allows for achieving specific conductance states. This exploration will promote the development of low-power, high-precision, and area-efficient devices based on graphene monolayer for various ANNs applications.

5.2. Monolayer-TMDs-Based Planar Memtransistor

The aforementioned planar FET-type memtransistor with three-terminals exhibits the effects of multilevel memory on a device unit.[33] However, it still face challenges in achieving complex neural functions such as heterosynaptic plasticity; hence, RS devices with more terminals are required.[48] In recent years, memtransistors based on monolayer MoS_2 have been reported.[35,48–50] In general, these memtransistors were fabricated based on the single-layer polycrystalline MoS_2 grown on different substrates via chemical vapor deposition (CVD) method. Sangwan et al. reported the successful fabrication of gate-tunable six-terminal memtransistors with heterosynaptic functions based on a MoS_2 monolayer.[48] A monolayer MoS_2 memtransistors array is shown in **Figure** 5a. A schematic of the planar memtransistor unit is also illustrated (Figure 5b). At a V_D (drain bias) below the threshold voltage (80 V) and with a certain gate bias, the MoS_2 memtransistor was initially in a high resistance state (HRS) and gradually switched to a low resistance state (LRS) ($V_D > 80$ V). The device retained the LRS until it was reset to the HRS; consequently, this device exhibits the LRS–HRS memtransistor behavior (Figure 5c). The I_D–V_D characteristics of the device with different V_G are also illustrated (Figure 5d). As shown in Figure 5e, the endurance of the MoS_2 memtransistor is only ≈500 full-switch cycles. To study the origin of the RS behavior in this device, a phase image (Figure 5f) was acquired using electrostatic force microscopy (EFM) to provide a local potential map of the device. The line profiles of the in situ EFM phase indicate a higher contact resistance at the HRS than at the LRS. Similarly, the reverse-biased HRS likewise exhibits a larger potential drop in the drain region than the reverse-biased LRS, although the discrepancy is narrow, which is consistent with the lower ON/OFF ratio at the reverse voltage. The EFM results demonstrated that the switching mechanism in this memtransistor may have resulted from the height variation of the Schottky barriers at the source (drain) electrode. One advantage of planar memtransistors is that they allow the implementation of multiterminal neural circuits which can imitate multiple synaptic links in neurons. In a multiterminal planar memtransistor, the electrical conductivity among the inner electrodes (terminals 1–4) can be stimulated by sweep pulses applied to the outer electrodes (terminals 5 and 6), as the inner terminals are isolated (Figure 5g). Moreover, these planar MoS_2 memtransistors also permit the tuning of the heterosynaptic plasticity property through a gate electrode. Plasticity and long-term memory were also observed (Figure 5h), which can be used to mimic the stimulating and depressing synapses of organisms via the duplication of reversed bias pulses (Figure 5i).

The underlying resistive switching mechanism for these gate-tunable planar memtransistors is possibly related to the process of defect migration between the GB and depleted regions (drain/source electrode region).[49] Mobile Mo cations are less likely to exist in MoS_2 memtransistors;[51] therefore, the sulfur vacancies are the most probable candidates for mobile defect species within the MoS_2 atomic sheet.[49] In fact, studies indicate that the sulfur vacancies in MoS_2 accumulate near the GB.[52] In a previous study, EFM and spatially resolved photoluminescence spectroscopy indicate that sulfur vacancies migrate from the GB to the depleted region during the SET process, thus changing the Schottky barrier and turning the memtransistor ON. Conversely, in the RESET process, the sulfur vacancies are driven away from the drain electrode and toward the GB region; consequently, the conductance is reduced and the OFF state is achieved.[49]

Compared to the single-layer graphene based memtransistor,[33] the monolayer MoS_2 memtransistor exhibits gate-tunable resistive memory behavior with more terminals.[48] However, the operating voltage is still relatively high. This technique provides an opportunity for the implementation of complex neuromorphic computing by simulating organismal neurons with multisignal response.

6. Application of 2D Monolayer Materials in Vertical Resistive Memory Device

6.1. Monolayer-TMDs-Based Vertical Atomristor

The multiterminal memtransistors based on monolayer 2D materials have the advantage of achieving complex neural functions, such as heterosynaptic plasticity.[48] However, vertical two-terminal MIM memristor devices are preferred for practical

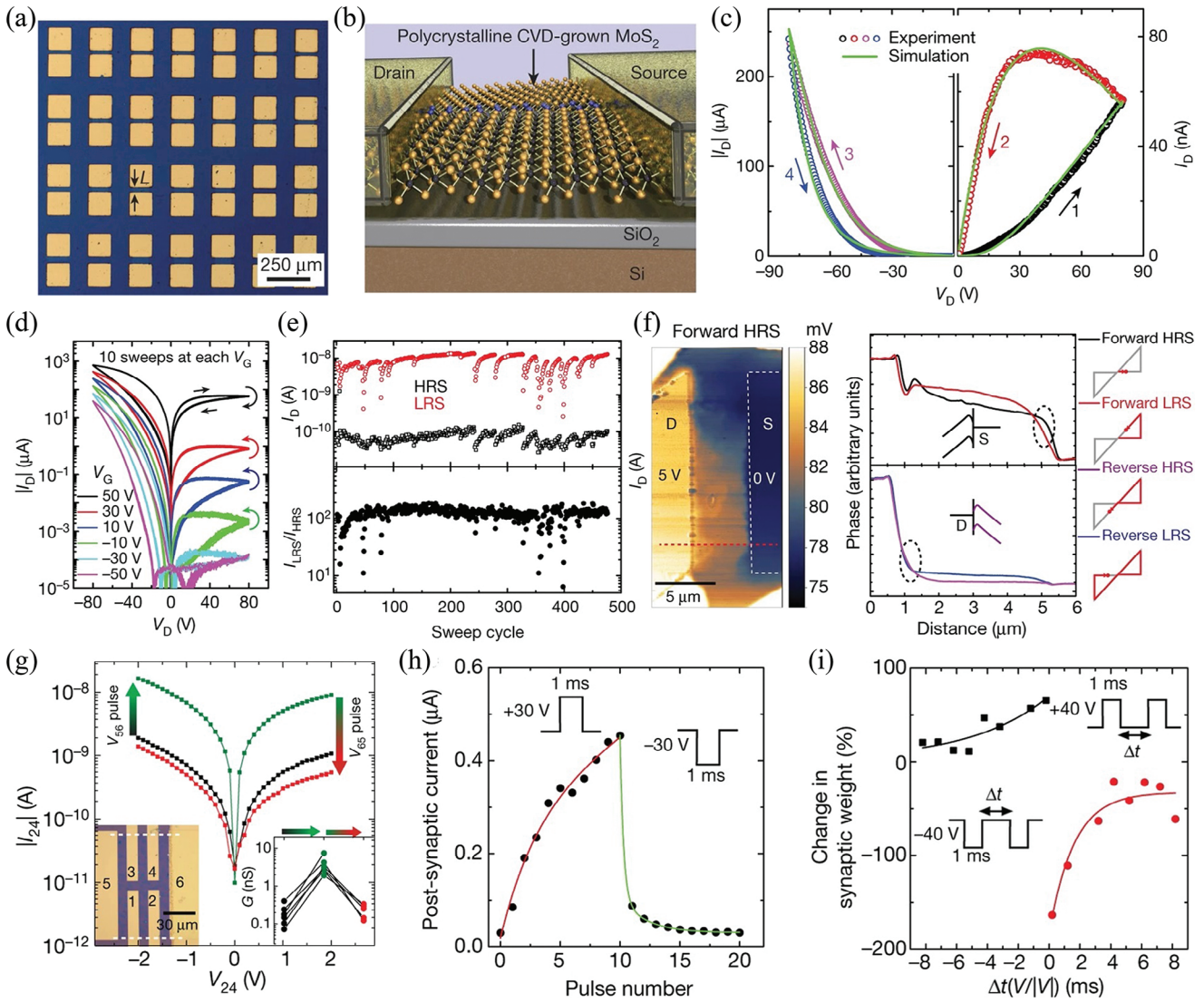

Figure 5. Architecture and characteristics of monolayer MoS_2 based memtransistor. a) Optical image of the manufactured monolayer MoS_2 memtransistors with different channel lengths (L). b) Illustration of a planar MoS_2 memtransistor unit fabricated on SiO_2 with doped Si as the gate. c) Measured I_D–V_D characteristics of a monolayer MoS_2 based memtransistor at $V_G = 10$ V. d) I_D–V_D characteristic of a device for 10 consecutive sweeps at different V_G. e) Variations in current (top) and I_{LRS}/I_{HRS} (bottom) versus endurance cycles at $V_D = 0.5$ V for the MoS_2 memtransistor for 475 switching cycles with $V_G = 40$ V. f) Electrostatic force microscopy (EFM) phase micrograph at initial high resistance state (HRS) of the MoS_2 memtransistor. EFM phase contour outlines along the steps as: forward-biased HRS, forward-biased low-resistance state (LRS), reverse-biased HRS, and reverse-biased LRS. g) Current–voltage curves (I_{24}–V_{24}) between ports 2 and 4 of a planar MoS_2 memtransistor with six-terminals (left inset) at different stages with $V_G = 20$ V. h) Postsynaptic current variations with pulse number under 30 and −30 V, presenting long-term potentiation and depression. i) The change of synaptic weight varied with time interval (Δt) using 40 and −40 V paired pulses. Reproduced with permission.[48] Copyright 2018, Springer Nature.

semiconductor technology because of their smaller footprints and easier integration.[36] 2D RRAM with vertical MIM structures is considered a promising candidate for the computing devices because it can simultaneously achieve low-power memory and computational operations.[53] Over the past several years, NVM switching has been demonstrated in a series of typical multilayer 2D materials in the vertical direction, such as black phosphorus,[54] transition metal dichalcogenides (TMDs),[50,55,56] and *h*-BN,[57–59] in which the HRS and LRS can be switched by the reversible formation and rupture of conductive filaments. Over the years, the MIM structure of 2D monolayer materials were regarded as having no NVM switching phenomenon because of the significantly large leak current. However, researchers have recently observed the NVM behavior in monolayer TMDs or *h*-BN based vertical devices[36,38,60] and named them as atomristors. Subsequently, other researchers also demonstrated similar NVM switching effects in these atomic-sheet devices.[61,62]

The monolayer 2D materials used for vertical memristor applications can be divided into two categories. One uses an atomic sheet with sublayers, such as TMDs, whereas the other employs a one-atom-thin sheet, such as *h*-BN. Typically, the standard or metal-organic CVD methods are used for the synthesis of TMDs

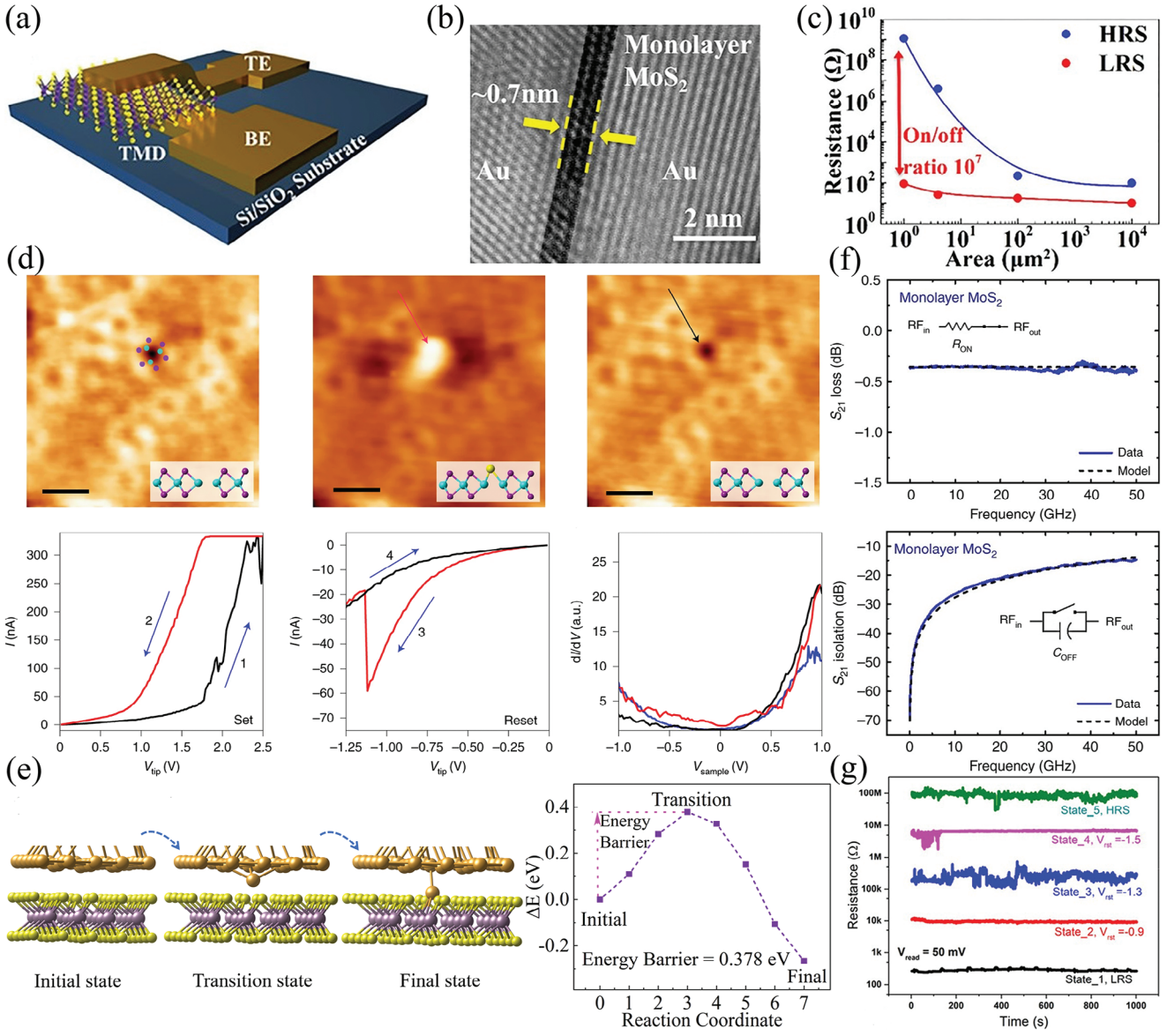

Figure 6. Working principles and characteristics of monolayer TMDs based atomristor. a) Schematic of metal–insulator–metal (MIM) structures of monolayer TMDs based memristor. b) Cross-sectional TEM image of Au/MoS_2/Au atomristor unveils the high-quality atomic interface. c) LRS and HRS area-dependence characteristic of MoS_2 atomristor. a–c) Reproduced with permission.[36] Copyright 2018, American Chemical Society. d) Observation of adsorption and desorption processes of Au atom on the surface of monolayer MoS_2 and scanning tunneling spectroscopy (STS) measurements on V_{S2} defect before (black) and after (red) Au adsorption. Blue curve is the STS curve that was taken far away from the defect point. Reproduced with permission.[63] Copyright 2021, Springer Nature. e) Simulated atomic pictures of an Au atom dissociating from top electrode and being adsorbed on the V_S vacancy in MoS_2. The energy barrier is 0.378 eV. Reproduced with permission.[64] Copyright 2023, IOP. f) Measured S-parameter in SET (insertion loss) and RESET (isolation) state of a MoS_2 atomristor based radio-frequency (RF) switch with a size 0.5 × 0.5 μm^2. The extracted values of R_{ON} (ON-state resistance) and C_{OFF} (OFF-state capacitance) were 4.2 Ω and 6.5 fF, respectively. Reproduced with permission.[65] Copyright 2018, the authers. Published by Nature Publishing group under a Creative Commons Attribution 4.0 International License (CC BY 4.0). g) Time-retention stability of the multilevel resistance states observed experimentally in the monolayer MoS_2 based atomristor. Reproduced with permission.[61] Copyright 2020, American Chemical Society.

atomic sheets.[66,67] Akinwande et al. fabricated an MIM atomristor based on a transferred monolayer MoS_2 (**Figure 6a**) and then explored the device performance and resistive switching mechanism.[36,63,65] Transmission electron microscopy (TEM) is employed to visualize the cross-sectional morphology of the manufactured MIM (Figure 6b). An abrupt and clean interface is observed between the dielectric layer and the electrodes, which guarantees the HRS of the atomristor. The thickness of the MoS_2 sheet is merely 0.7 nm. Bipolar resistive switching behavior is observed via DC electrical measurements; the SET voltage is ≈1 V, whereas the RESET voltage is ≈1.25 V. The atomristor switching does not require an electro-forming process. The area-dependent

characteristics of the LRS and HRS indicate that a high ON/OFF ratio (≈10^7) can be achieved (Figure 6c) for these atomristors. The endurance test results show that the MoS_2 atomristor could tolerate only 150 DC switching cycles.[36] Although the MoS_2 atomristor exhibits superior performance in this work, its endurance must be significantly improved for practical applications.

The reason for the nonvolatile resistive switching (NVRS) property in these atomic devices is also explored recently; for example, analyses are performed via scanning tunnelling microscopy or scanning tunnelling spectroscopy (STM/STS).[63] As shown in Figure 6d, the monolayer MoS_2 is initially in HRS with a S vacancy defect (V_S) or a double S vacancy (V_{S2}). When a SET operation is induced by applying a voltage of ≈1.8 V, an LRS is realized. The STM image acquired in situ after the SET operation shows that the gloomy spot is superseded by a bright projection, indicating that the vacancy has been filled by an adsorbed Au atom. In situ STS measurements of the SET state exhibited a nonvanishing tunneling signal around the Fermi level, exposing the conduction character of the Au-adsorbed state. When an opposite voltage of −1.1 V is applied, a RESET event occurs. Succeeding in situ STM measurements indicate that the vacancy returns to its pristine state and the Au atom disappears. This study demonstrates that the switching mechanism of atomristors based on atomic sheets with sublayers is dominated by the adsorption and desorption processes of electrode atoms on vacancies of monolayer 2D materials.

To understand the switching process at the atomic scale, density functional theory (DFT) combined with Keldysh nonequilibrium Green's function (NEGF) theory are applied to study the resistive switching mechanism in a MoS_2 based atomristor.[64] As seen in Figure 6e, the Au atom from the top electrode tends to interact with a V_S nearby and be adsorbed onto it. Thus, a conductive filament is formed. The energy barrier of this process was reasonable as 0.378 eV. A similar switching process should also be applicable to the other TMDs (such as WSe_2 and $MoTe_2$) based atomristors. This process is consistent with the experimental observations.[60,63] This investigation provides an atomic picture of the resistive switching mechanism in theory and promotes the comprehension of these devices at the atomic scale.

Owing to the metallic conductive channel and high-quality single-layer crystalline material, in a prior study, the value of resistance is lower than 10 Ω when LRS is set, indicating the potential application in low-power radio-frequency (RF) switches of MoS_2 atomristor.[65] Owing to their nonvolatility, MoS_2 atomristor switches can consume zero-static energy, overcoming the disadvantages of traditional RF switches based on transistors or mechanical devices, which must dissipate both dynamic and static energy. The RF characterization of MoS_2 switches exhibits outstanding performance in terms of insertion loss (≈−0.3 dB) in the LRS and isolation (≈−10−20 dB) in the HRS up to 50 GHz (Figure 6f). Moreover, as $f_c \propto 1/C_{OFF} \propto 1/A$, the cutoff frequency ($f_c$) of the device can reach up to 100 THz when the A (device dimensions) <0.01 μm^2 owing to the low C_{OFF} (OFF-state capacitance).[65] Excellent high-frequency performance exhibited by switches based on the atomristor is helpful for developing an RF device for future communications.

Multilevel resistances are also observed in the monolayer MoS_2 based atomristor with MIM structures (as seen in Figure 6g).[61] Conductive atomic force microscopy is performed to study the transport properties in the vertical direction. In the initial state, the area is predominantly insulating, excluding some highly localized regions or hotspots with enhanced conductivity. After the SET operation, the density and size of the hotspots increase sharply, indicating an increased current intensity. After the RESET operation, many of the hotspots disappear, resulting in a reduced conductivity. Single-crystalline MoS_2 is chosen for this experiment, and the results demonstrate that the NVRS characteristics of these atomic devices are not necessarily dependent on the grain boundaries. The multilevel resistances observed here may pave the way for the application of two-terminal atomristors in neuromorphic computing.

Owing to the large variations among different atomristors, the in-memory computing based on these atomic devices is still lacked over the years.[68] Until most recently, an all-atomristor logic gates based on MoS_2 atomristor crossbar arrays are reported.[68] In this work, all-atomristor AND and OR gates are constructed under a memristor ratioed logic configuration and they exhibit logic computing ability, which is further verified by constructing a half adder consisting of only atomristors. Moreover, the function and performance of these logical gates in a crossbar structure are assessed using modeling analysis.[68] This investigation demonstrates the feasibility of using an atomristor for digital computing and data processing and provides opportunities for the development of in-memory computing technology based on atomristors.

Because the atomristors based on monolayer MoS_2 have predominantly been investigated at the present stage, we primarily focused on its RS properties.[64] In fact, in addition to MoS_2, the NVRS characteristics has been observed in a library of monolayer TMDs (MX_2, M = Mo, W, Sn; and X = S, Se, Te) materials.[60] However, systematic investigations for the device performance based on these TMDs monolayers are still lacking. It has been reported that in a $ReSe_2$ atomristor an endurance of 200 DC cycles is observed,[69] which is higher than that of a MoS_2 atomristor (150 DC cycles).[36] In addition, according to theoretical analysis, an atomristor based on monolayer WSe_2 is expected to have a larger ON/OFF ratio than that of a MoS_2 atomristor.[64] Hence, whether a memristor based on other monolayer TMDs will present better RS performance than that based on monolayer MoS_2 is also an important topic that deserves further investigations.

6.2. Monolayer-*h*-BN-Based Vertical Atomristor

As another typical 2D monolayer material, monolayer *h*-BN has the bandgap as high as 6.61 eV,[73] and its high insulating property prevents its application in planar memtransistors. Hence, its application is primarily focused on vertical atomristor. As one of the thinnest 2D materials, the single-layer *h*-BN exhibits a thickness of 0.33 nm.[38] Generally, monolayer *h*-BN atomic sheets are synthesized on metal foils using CVD method.[38,40,41] Then, the atom sheets are transferred onto SiO_2/Si substrates using a wet or dry transfer method to fabricate crossbar atomristor devices (**Figure 7a**). As seen in the measured *I*–*V* curves of the monolayer Au/*h*-BN/Au MIM crossbar device (Figure 7b), both bipolar and unipolar NVRS behaviors can be observed, and the operation voltage is relatively high for the SET process. The coexisting

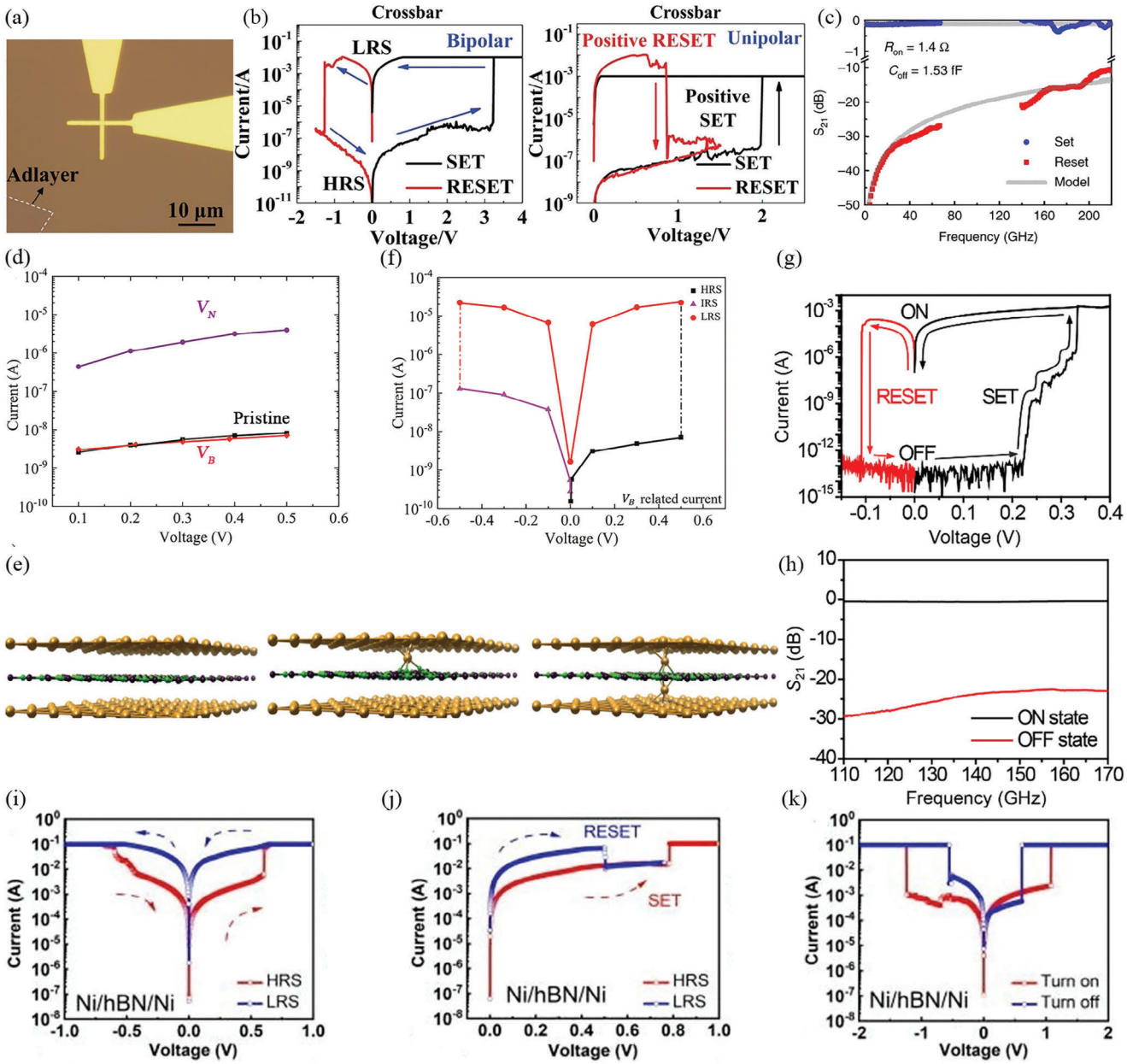

Figure 7. Working principles and characteristics of single-layer *h*-BN based atomristor. a) Optical image of the crossbar for Au/*h*-BN/Au atomristors. b) Bipolar and unipolar characteristics of *I*–*V* curves measured in the *h*-BN atomristor crossbar with 1 × 1 μm^2 size. a,b) Reproduced with permission.[38] Copyright 2019, John Wiley & Sons. c) Measured S-parameter (S_{21}) and fitting line of the Au/*h*-BN/Au atomic RF switch up to sub-terahertz range. The ON and OFF states are observed with 0.5 × 0.5 μm^2 and 0.25 × 0.25 μm^2 size devices, respectively. Reproduced with permission.[70] Copyright 2020, Springer Nature. d) Theoretically calculated *I*–*V* curves of pristine and defective *h*-BN in vertical Au/*h*-BN/Au atomristors. e) Atomristor is in HRS without filament, intermediate resistance state (IRS) with semiconductive filament, and LRS with full conductive filament. f) Calculated *I*–*V* curves for each state of the atomristor. d–f) Reproduced with permission.[71] Copyright 2022, AIP. g) *I*–*V* curves and h) RF switching characteristics of the Ag/*h*-BN/Ag device. g,h) Reproduced with permission.[72] Copyright 2023, American Chemical Society. i–k) Bipolar resistive switching (BRS), unipolar resistive switching (URS), and threshold switching (TS) behaviors in Ni/*h*-BN/Ni device. i–k) Reproduced with permission.[42] Copyright 2022, AIP.

bipolar and unipolar characteristics indicate that the RESET process in this atomically thin memristor should be dominated by thermal effects. When the device is fabricated on a polycrystalline diamond substrate with a high thermal conductivity that is > 1000 W m^{-1} K^{-1}, the monolayer *h*-BN atomristor also exhibited excellent high-frequency performances owing to the low values of both R_{on} and C_{off}.[70] The measured inherent RF properties of the Au/*h*-BN/Au atomristor exhibit a low insertion loss at LRS of ≈−0.27 dB and isolation of ≈−35 dB at HRS with significantly high frequencies of 67 GHz. By further improving the test frequency, the superior characteristics could be maintained up to 220 GHz, which falls within the sub-terahertz range. The switch

still exhibited a low insertion loss (≈−0.5 dB) and good isolation (≈−10 dB) (Figure 7c). Compared to the monolayer MoS_2 atomristors, *h*-BN switches exhibit lower insertion loss and higher isolation, indicating promising applications in 5G and terahertz communication systems.

These findings successfully scale the size of memristor down to the atomic thickness in the vertical direction. Although the stability of these atomristors must be further improved, they provide a new approach for developing ultradense atomic memory and zero-static power RF switches.

Previous reports have demonstrated that the NVRS behavior in these atomic devices is related to the adsorption–desorption process of the electrode atoms.[38,63] The conductive mechanism of *h*-BN atomristor is still being debated. Recently, a DFT calculation combined with NEGF method is employed to investigate the working mechanism of Au/*h*-BN/Au atomristor.[71] The calculated *I*–*V* curves, as shown in Figure 7d indicate that the atomic sheet with V_B could maintain good insulation characteristics, similar to those of pristine *h*-BN. However, the *h*-BN with V_N exhibits a large leakage-current, which hinders its use as a dielectric layer for atomristor. Hence, the resistive switching process in the monolayer *h*-BN based atomristor is probably related to V_B. The migration process of metal atom is also evaluated, and the energy barrier for an Au atom passing through *h*-BN via V_B is determined to be reasonable and as low as 0.832 eV. Consequently, it is proposed that the metal atom from electrode can penetrate the atomic sheet via V_B to form a fully conductive filament for an effective LRS in the *h*-BN atomristor. As seen in Figure 7e, the state of just an Au atom adsorbed to V_B is an intermediate resistance state (IRS). The *I*–*V* curves for each state of the atomristor are then calculated. Figure 7f shows that the current for the IRS is merely one order of magnitude larger than that for the HRS at the same voltage. In fact, it still cannot achieve the observed 10^3 ON/OFF ratio in the experiments.[38] However, the current for V_B pinning Au-full-filament can reach up to three orders of magnitude higher than that in the HRS. The molecular dynamics simulation further demonstrates that the nonvolatility or stability of this atomic conductive filament can be retained at least up to 500 K.

This investigation provides a critical atomic picture for the conductive mechanism in an atomristor at the thinnest limit, which is significant for atomic device design. The intermediate resistance state proposed here will also promote a precise resistance control in atomristors. However, the migration of electrode atoms under an electric field still requires further investigations.

To sum up, the resistive switching mechanisms for these ultrathin vertical memristors, lateral memtransistors, and atomic threshold switches should be dependent on the interactions between the defects in the 2D monolayer materials and metallic atoms in the electrodes.[41,49,63] For instance, in a vertical memristor, the RS behavior is resulted from the adsorption process of electrode-metal atoms on the vacancy defects in the atomic layers;[63] and in lateral memtransistors the RS behavior is related to the migration process of defects in 2D monolayers, which will lead to a change in the Schottky barrier at the source (drain) electrode.[49] The switching mechanisms of these atomically thin layers are indeed different from the cases of the 2D multilayer materials. For instance, in a vertical memristor based on 2D multilayer materials, the conductive filament is considered to be formed by the assistance of a grain boundary,[57] whereas in a memristor based on a 2D monolayer, the conductive filament is formed via a point defect.[71]

In addition to the aforementioned symmetric Au electrodes, *h*-BN atomristors with different electrodes are also investigated.[42,72] An atomristor with Ag electrodes (Figure 7g,h) exhibits significantly higher ON/OFF ratios of up to 10^{11}, and the SET voltage is lowered to 0.34 V, which is significantly advantageous when compared to the atomristor with Au electrodes.[38] Meanwhile, the device also has excellent RF characteristics and can be used in the sub-terahertz range. However, the power consumption for the SET process is 1.2 nJ in this device, which is still high.

Atomristors with symmetric Ni/Ni electrodes exhibit the coexistence of bipolar resistive switching (BRS), unipolar resistive switching (URS), and threshold switching (TS) behaviors, as seen in Figure 7i–k. Under the BRS conditions, the SET and RESET voltages are almost identical in the symmetric Ni/*h*-BN/Ni devices, whereas in the asymmetric devices (Au or Pt/h-BN/Ni), the SET voltages are usually larger than the of RESET voltages. This interesting phenomenon indicates that a built-in electric field exists in asymmetric devices, which is due to the differences in the metal work functions.[42] However, the reason why the BRS, URS, and TS phenomena can coexist in these atomristors remains unclear. The point at which the device can switch between nonvolatility and volatility is also unknown. These issues require further investigations. The diversity of the resistive switching behaviors observed in *h*-BN atomristors indicates their potential for future RRAM applications.

6.3. Performances of Monolayer-2D-Materials-Based Memristors

To objectively evaluate the performances of monolayer-2D-materials-based memristors, the key performance parameters of these atomic devices are summarized in **Figure 8**. Currently, the thickness of metal oxide in resistive switching devices can be scaled down to ≈5 nm, whereas the thickness of 2D materials can easily fall below 3 nm. Owing to the atomically thin characteristic, the thickness of monolayer TMDs is only ≈0.7 nm,[36,61] whereas the one-atom-thin *h*-BN sheet has a thickness of ≈0.33 nm.[38]

Although 2D monolayer material based memristors exhibit the inherent advantage of atomic thickness, their operating voltages are currently higher than those of metal oxide and multilayer 2D materials based memristors (Figure 8a). The SET voltages for metal oxide and multilayer 2D materials based memristors can reach ≈0.5 V, whereas those for most monolayer 2D materials based memristors are larger than 1 V. According to International Technology Roadmap for Semiconductors (ITRS), the technological requirements for RRAM should be below 1 V.[32] At the present stage, the memristor based on monolayer 2D materials are primarily adopted symmetrical and inert Au/Au electrodes.[36,38,61,62,69] That may be one of the reasons why higher SET voltages are required for these atomic devices. While we note that if the active electrodes (such as Ag/Ag) are adopted, the SET voltage of the device can be significantly lowered.[72] In addition, when asymmetric electrodes (such as Ni/Pt) are adopted, the SET voltage of the device is also lowered.[42] The

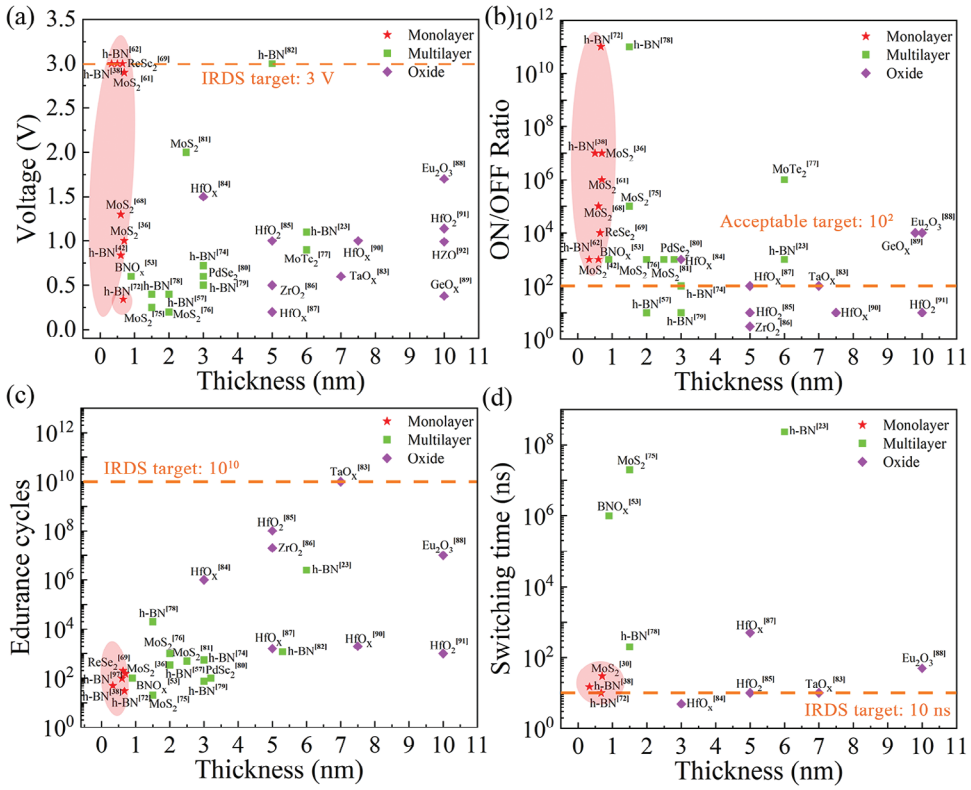

Figure 8. Performances of monolayer 2D materials based MIM memristors. Comparison plot of a) SET voltages, b) ON/OFF ratios, c) endurance cycles, and d) switching time (speed) versus thickness for certain memristors fabricated using typical 2D monolayers, 2D multilayers, and metal oxide materials.[23,36,38,42,53,57,61,62,68,69,72,74–92] The orange dashed line in the picture indicates the IRDS requirements for NVM,[46] note that the ON/OFF ratio is not a strictly defined parameter but is generally considered as ≈10^2.[93] The datapoints of the memristors based on 2D monolayer materials are highlighted by the pink background.

ON/OFF ratio of monolayer 2D material based memristors can reach up to 10^7, which is excellent among these nanomemristor devices (Figure 8b). Conversely, the ON/OFF ratios of metal oxide and multilayer 2D materials based memristors are generally $<10^3$. Endurance is another important performance parameter for memristor devices. As seen in Figure 8c, the cycle numbers for metal oxide based memristors are ≈10^7, whereas the cycle numbers are ≈10^3 for the multilayer 2D materials based memristors. However, the cycle numbers for most monolayer-materials-based memristors are merely about 10^2 under a DC bias, which is insufficient for meeting the requirements of practical applications. Therefore, it is essential to investigate the failure mechanism in these atomically thin devices and find solutions for improving the endurance. It is worth noting that Nikam et al. reported a volatile resistive switching device based on monolayer *h*-BN with Ag/Pt electrodes having an endurance of 10^7 cycles with using AC pulses.[41] The reason for this large difference is probably related to the test method.[94] Hence, it is of importance to establish a measuring standard to evaluate switching endurance of these atomically thick resistive switching devices.[95] Switching speed is another important performance parameter for monolayer 2D material-based memristor. Its switching speed is faster than that of a multilayer 2D materials based memristor (Figure 8d). The switching time of monolayer 2D material-based memristor is close to that of metal oxide device. The switching time as fast as ≈15 ns can be achieved when a monolayer *h*-BN is sandwiched between two Au electrodes.[38] According to the ITRS, for a high integration density, the area of a MIM cell for RRAM should be smaller than 576 nm^2 (= 24 × 24 nm^2),[32] whereas the sizes of memristors based on monolayer 2D materials that have been reported till now usually range from 1 × 1 μm^2 to 3 × 3 μm^2. Thus, a wide gap exists between the sizes of these atomic devices and the ITRS requirement.[32,36,38,60,62,69] On the other hand, reproducibility and reliability are two important issues. In ref.[38] the RS characteristics of 15 devices based on monolayer *h*-BN are presented, and the SET voltages are varied from 2 to 3.5 V.[38] In ref.[62] the RS characteristics of 100 devices based on monolayer *h*-BN are presented, and the SET voltages are varied from 2 to 4 V.[62] The device-to-device variations are relatively large, whereas the specific values of the standard deviation are not presented in these studies. Currently, the smallest reported device area for a memristor based on monolayer 2D materials in crossbars is in several square micrometers. Although the results have also been reported by different research groups,[38,42,61,62,68,96] the yield of memristors based on monolayer 2D materials is only ≈5% at the present stage.[62] Hence, reproducibility and reliability remain as challenges for such ultrathin memristors.

According to the International Roadmap for Devices and Systems (IRDS), to integrate with current ICs, commercial NVM devices (such as RRAM, phase change memory (PCM), and NAND Flash) should meet the following requirements: writing voltages

<3 V, switching energy <10 pJ, switching time <10 ns, writing endurance >10^{10} cycles.[46] On the other hand, according to the ITRS, the requirements for RRAM devices are as follows: writing voltages < 1 V, writing endurance >10^9 cycles, and switching time <10 ns.[32] We have also displayed the targets from the IRDS in Figure 8 and compared them with the performances of 2D monolayer material-based memristor devices. At the present stage, commercial RRAM based on metal oxide has been demonstrated to have fast speed (<10 ns), large HRS/LRS resistance ratios (>100), low switching energy (<0.1 pJ), and relatively high endurance (≈10^6). Exploiting these performance parameters, Fujitsu has commercialized a low-power 8-Mb stand-alone RRAM chip, which can operate at 1.6 V with an average read current of 0.15 mA.[20,46,97] Compared to the aforementioned commercial RRAM and the requirements specified by IRDS/ITRS, memristors based on monolayer 2D materials have an endurance of just ≈10^2 under a DC bias at the current stage; there is a wide gap between the commercial requirement and their endurance performance. The operating voltage and switching speed of the atomristors (Figure 8) are close to those of the metal oxide RRAMs. However, these atomic devices possess the advantage of high ON/OFF ratios, which are typically >10^3.

In addition to the thickness of the channel layer, the performances of memtransistors are also determined by the channel length, gate voltage, as well as the number of terminals, it is difficult for these memtransistors to make a comparison. As for the threshold switching characteristic of monolayer 2D materials, it is mainly observed in single-layer *h*-BN at the present stage,[40–42] and the data are still too little. Hence, in this review, we focus on the performance comparisons of vertical memristors.

Some representative advancements in resistive memory switching devices based on 2D monolayer materials are also listed in **Table 1**. As the planar resistive switching device with two terminals is fabricated using the monolayer graphene,[44] for ease of application in future neuromorphic computing, the planar RRAM device based on 2D monolayer materials is being developed with more terminals and resistance levels. Moreover, the vertical resistive switching device based on 2D monolayer materials is being developed toward smaller device size for high density storage and RF switch applications. The same dielectric layer exhibits different performances when in different structures. Developing methods to match the 2D monolayer materials with suitable device designs for improving their performances will be an important issue in the near future.

7. Main Challenges

7.1. Endurance and Uniformity

The variability of these atomic devices includes two aspects: device-to-device variation (among different cells) and cycle-to-cycle variation (within the same device) of the electrical characteristics (**Figure 9a**). Though the variability characteristic may be helpful for developing specific devices for security applications,[99] typically, RRAM devices with high reliability and low device-to-device variability are preferred. Maintaining consistency in device-to-device and cycle-to-cycle performance is a precondition for promoting 2D monolayer materials based resistive switching devices for industrial applications. Therefore, it is of great importance to improve consistency of these atomic devices. On the other hand, the reliability of these atomic RRAMs needs more demonstrations. Currently, the yield of a memristor based on monolayer *h*-BN is only 5%, whereas that of a device based on multilayer *h*-BN can reach up to 98%.[59] As the development of these atomic device based on 2D monolayer materials is in its nascent stage, controlling the fabrication technology more precisely is expected to improve the yield of these atomic devices. Endurance is another significant issue associated with these devices. In particular, the cycle numbers of monolayer *h*-BN and MoS_2 based RRAMs were merely ≈10^2 under DC voltage sweeps.[36,38,61] Moreover, the origin of device failure has not been well understood. In near future, developing more stable material systems and finding solutions to improve the endurance and uniformity are important tasks for researchers.

According to the relationship between the endurance of vertical memristors and the device size, it is indeed that the devices with thinner dielectric layers and smaller areas will suffer from a reduced endurance. The accumulation of metal atoms should be one of the reasons leading to the poor endurance of these thinner memristors.[19] In general, a higher forming voltage is required for a smaller device area.[45] In these thinner dielectric materials the effect of defects will be amplified.[19] When larger-size defects exist in these 2D monolayers, a higher voltage applied to the device will trigger the accumulation of metal atoms via the larger-size defects and then the short-circuit effect,[45,71] thereby reducing the endurance.[45] On the other hand, the high adsorption energy between the vacancies (in monolayer 2D materials) and the electrode metal atoms[64,71] may also be disadvantageous for triggering the RESET process in these atomristors, resulting in poor endurance. Hence, the following suggestions may be helpful for improving the endurance of these atomic devices. 1) larger-sized defects (such as V_{BN} or voids in *h*-BN monolayer) should be avoided via defect engineering[100,101] when monolayer 2D materials are grown for atomristor applications. 2) New conductive mechanisms, such as those that avoid the formation of metallic filaments, should be developed to prevent metal atoms from participating in the resistive switching process.

7.2. Resistive Switching Mechanism

The conductive mechanism in these 2D-monolayer-materials-based resistive switching devices is complex. The switching behavior should involve interactions among defects, electrons, metal ions, interfaces, and even grain boundaries, as seen in Figure 9b. At the present stage, it is difficult to peer into an atomic device and completely uncover the physical processes of resistance switching. Investigating whether a nonconductive-filament mechanism exists in these atomically thin devices will be worthwhile. The concept of electron tunneling through these atomically flat materials remains intricate.[38,61,102] The different 2D monolayer materials based RRAMs may have different conductive mechanisms depending on the device structure,[36,48] properties of dielectric layer (bandgap, trap energy level, etc.),[38,61] and the interface between the monolayer and metal electrodes.[103,104] The same atomic sheet exhibits different tunnelling processes under different bias voltages.[102] In addition, the migrations of metal atoms[63] and vacancies[35] would trigger a change in the

Table 1. Summary of certain representative progresses of resistive memory devices realized with 2D monolayer materials.

Year	Device structure	Finding	Performance	Refs.
2008	Planar	Fabrication of monolayer graphene-based planar two terminal device	V_{SET} ≈2.5–4 V Switching speed ≈100 ms Endurance ≈500 cycles Multilevel (>4) resistances	[44]
2015	Planar	Discovery of gate-tunable memristive phenomena in single-layer MoS_2 based device with FET structure	V_{SET} ≈3.5–8 V ON/OFF ratio ≈10^3	[49]
2017	Planar	Fabrication of monolayer MoS_2 based FET-type memory on a flexible substrate	Endurance ≈8000 cycles ON/OFF ratio ≈10^4 the devices can be strained up to 1%	[50]
2018	Vertical	Discovery of nonvolatile vertical MIM atomristor based on TMDs monolayers	V_{SET} ≈1 V Switching speed ≈30 ns Endurance ≈150 DC cycles ON/OFF ratio ≈10^7	[36]
2018	Planar	Discovery of multiterminal planar memtransistors based on polycrystalline monolayer MoS_2	Endurance ≈475 cycles	[48]
2018	Vertical	Discovery of the excellent RF performance of vertical MoS_2 atomristor	f_c > 100 THz for nanoscale device	[65]
2019	Vertical	Discovery of the thinnest vertical MIM atomristor based on *h*-BN monolayer	V_{SET} ≈3 V Switching speed ≈15 ns Endurance ≈50 DC cycles ON/OFF ratio ≈10^7	[38]
2020	Vertical	Discovery of the multilevel (≈5) resistive switching in monolayer MoS_2 based vertical atomristor	V_{SET} ≈2.9 V ON/OFF ratio ≈10^6	[61]
2020	Vertical	Discovery of the excellent RF performance of *h*-BN atomristor	f_c ≈129 THz	[70]
2020	Planar	Discovery of graphene-based multilevel (>16) planar memristive synapses with arbitrarily programmable conductance state	Endurance ≈200 cycles	[33]
2021	Vertical	Observation of single-defect related adsorption and desorption process of monolayer MoS_2 based vertical atomristor	Control of the resistive switching of a single-defect	[63]
2022	Vertical	Discovery of atomic threshold switch based on monolayer graphene and *h*-BN heterostructures	V_{SET} ≈0.6 V Switching speed ≈70 ns Endurance ≈10^4 AC cycles ON/OFF ratio ≈10^8	[40]
2022	Vertical	DFT discovery of single-defect related Au penetration process and full atomic conductive filament of monolayer *h*-BN based vertical atomristor	ON/OFF ratio ≈10^3 Stability of the atomic conductive filament up to 500 K	[71]
2023	Vertical	MoS_2 all-atomristor logic gates were fabricated	VSET≈1.3 V ON/OFF ratio ≈10^5	[68]

interface barriers during the switching process. Details of the physical mechanism of electronic transport in the resistance switching process of these atomic devices remain a critical topic.

Computational simulation seems to be an important method for investigating the resistive switching mechanisms in these atomic devices. However, owing to the limitations of the computing scale of the ab initio method, computing the properties of a complete device model is currently challenging. A reasonable simplification of the atomic model is worth discussing. The reactive force field (ReaxFF) method, which can model chemical reactions such as bond breaking and forming with an accuracy close to that of DFT,[105] is a promising path for stimulating the evolution of conductance channels under electric fields in these atomic devices. Therefore, it is import to develop ReaxFF potential for RRAM materials system. Machine learning can be used to predict performances, and screen new materials or device architectures for monolayer 2D material based RRAM devices; however, the relationship between material properties and device

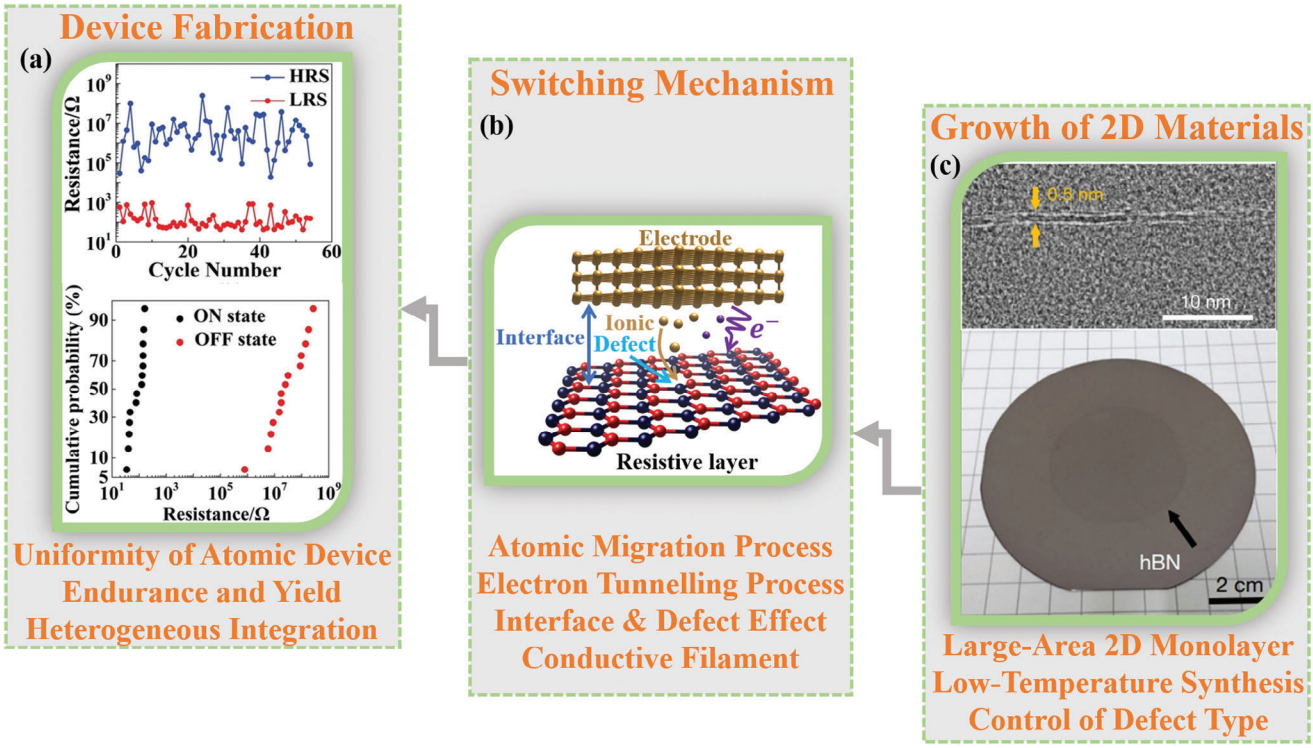

Figure 9. Main challenges of monolayer 2D materials based resistive memory devices. a) Resistance distribution collected from 15 *h*-BN atomristors at their LRS and HRS, and endurance of *h*-BN atomristor with just ≈50 DC switching cycles. Reproduced with permission.[38] Copyright 2019, John Wiley & Sons. b) Schematics of switching behaviors in these atomic devices involves interactions among defects, electrons, metal ions, and interfaces. c) Cross-sectional TEM image of a monolayer *h*-BN transferred onto SiO_2/Si with thickness of ≈0.5 nm, and a photograph of 2 in. monolayer *h*-BN film transferred onto a four-inch SiO_2/Si wafer. Reproduced with permission.[98] Copyright 2020, Springer Nature.

performances is still unclear. Another difficulty is how to simulate the functions for these atomic devices in a quantum mechanical accuracy. In fact, the resistivity in these devices is changing under different bias voltages owing to the dynamic changes in the structures.[61] However, at the present stage, simulations of *I*–*V* curves for these atomic RRAM devices are usually based on static structures using the NEGF method.[38,61,71] It is still difficult to automatically calculate the dynamic evolution of *I*–*V* curves according to the atomic motions during the switching processes while fully considering various transport effects. Hence, exploring suitable methods to simulate the functions of monolayer 2D materials based RS devices at the atomic scale is an important direction for future research.

7.3. Growth of Monolayer 2D Materials and 3D Monolithic Integration

In general, the CVD method is used to synthesize high-quality and large-area monolayer 2D materials, such as *h*-BN,[98] graphene,[39] and TMDs.[106–108] The issue is that the reaction condition for growing is typically above 700 °C, which blocks the direct synthesis of the atomic sheet on wafers with existing integrated circuits technology owning to diffusion problems.[109] The highest temperature to which the current CMOS integration can be exposed is 450 °C.[110] One solution is to develop a low temperature synthesis method and directly integrate the monolayer 2D materials-based devices into arrays. However, achieving low temperature growth of high-quality monolayer 2D materials on industrial substrates is currently difficult.

3D monolithic integration is a technology that can integrate memory devices and transistors at a higher density by increasing the number of 3D layers and reducing the parasitic interconnect resistances.[111–114] Although the transfer of materials is a practical way to achieve 3D monolithic integration of monolayer or multilayer 2D materials, cracks, wrinkles, and impure particles produced during the transfer process will lead to a change in resistance of these RRAM devices.[62] To apply the monolayer-2D-materials-based atomristors/memtransistors in complex neuromorphic computing, appropriate methods must be developed for transferring monolayer 2D materials at the wafer scale without introducing new defects and achieving large-scale integration (as presented in Figure 9c).

8. Conclusions and Perspectives

Studies on resistive memory devices at the thinnest limit based on monolayer 2D materials have begun in recent years. As single-layer 2D-materials-based resistive memory devices are being developed for better performances and more complex functions, 2D monolayer materials will play an important role in future electronic technologies, such as data storage/memory, RF switches, in-memory computing, and neuromorphic computing. However, research and development of 2D monolayer materials based

resistive memory devices is still in the early stages. Although their RS devices have the advantages of a high ON/OFF ratio and fast switching speed, critical challenges such as poor endurance and low yield still need to be addressed before these devices can meet the standards for commercial applications. To overcome these challenges, the defects of these thinnest materials and electrode metal atoms should be precisely controlled, and innovative RS devices, such as atomristors based on nonfilament conductive mechanisms, should be considered.

Acknowledgements

This work was supported by the National Key R&D Program of China (Grant No. 2022ZD0117600), the National Natural Science Foundation of China (Grants No. 12274172 and 12274180), and the Natural Science Foundation of Jilin Province (No. 20230101007JC). High Performance Computing Center (HPCC) at Jilin University is also acknowledged.

Conflict of Interest

The authors declare no conflict of interest.

Keywords

2D monolayer materials, atomristor, memristor, memtransistor, nonvolatile memory

Received: August 7, 2023
Revised: December 28, 2023
Published online:

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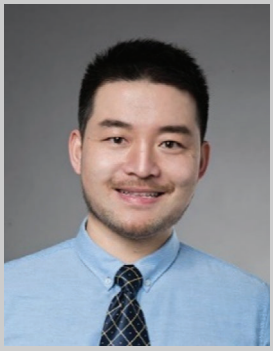

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